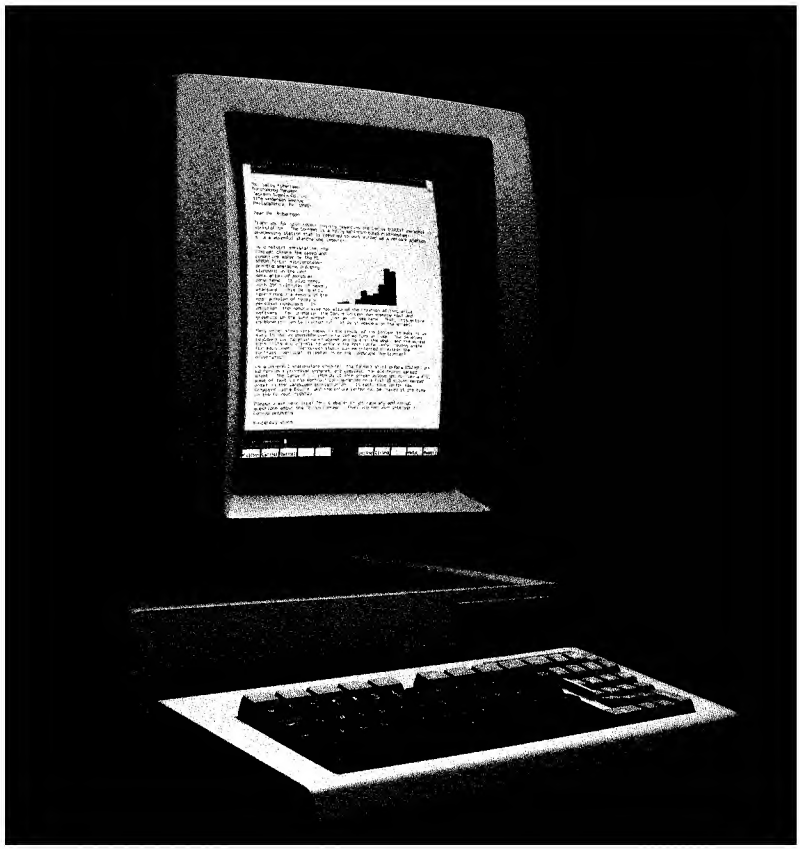
THE CORVUS SERVICE MANUAL



Corvus Concept

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CORVUS SYSTEMS
CONCEPT
PERSONAL WORKSTATION
SERVICE MANUAL

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RELEASE DATE: April, 1983

This document contains three types of notations. These are, in increasing order of importance. *NOTE,* **CAUTION,** and ***WARNING.*** The *NOTE* indicates some action to be taken to speed or simplify a procedure. The **CAUTION** indicates that potential damage to the equipment or user data exists, and care should be taken to avoid this. The ***WARNING*** indicates that potential harm or injury to the service technician or operator exists, and extreme care should be taken to avoid these.

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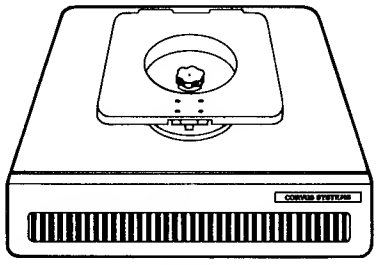
CHAPTER 1
OVERVIEW

1.0 Scope of Chapter

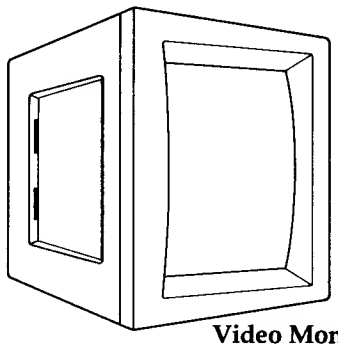
The Corvus Concept™ Personal Workstation™ is designed with service in mind. Its modular components can be substituted during on-site servicing to minimize system down time. These modules are outlined in this chapter. Options available to enhance the Concept are also discussed.

1.1 Concept Modules

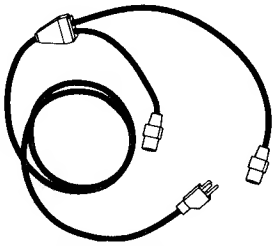
The Concept base contains a power supply, fan, and removable electronics tray. This tray contains the Processor Board, the Memory Board, speaker, and calendar battery. The modular design of the Concept allows easy access and replacement of the electronic subassemblies.



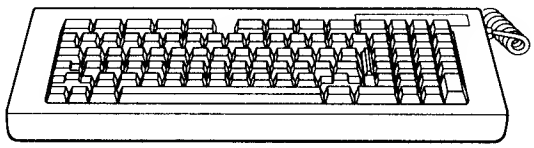
Base



Video Monitor



Bifurcated Cable



Keyboard

1.1.1 Electronics Tray

The entire tray may be removed for replacement when an immediate repair is required. The Processor Board and Memory Board may be individually substituted if time permits additional troubleshooting.

1.1.1.1 Processor Board

A Motorola™ MC68000 Microprocessor, Boot RAMs and ROMs, OMNINET,™ and Clock Calendar are the major components of the Processor Board. I/O circuitry is also resident on the Processor Board. Specific features include:

Microprocessor

- Motorola MC68000
- 16/32-bit data registers
- 24-bit memory address bus
- 16-bit data bus

Input/Output

- OMNINET Network interface
- Two serial asynchronous I/O ports
- Clock and calendar backup battery
- Flexible sound generator
- Two interval timers
- Four 50-pin I/O slots

1.1.1.2 Memory Board

The Memory Board provides a sophisticated scheme which produces both memory timing and video timing. The Memory Board includes:

- 256 Kbytes standard or 512 Kbytes optional memory
- Vertical and horizontal timing
- RAM timing
- Memory addressing
- Video interface
- System master clock

The 256 or 512 Kbytes is provided by 64K dynamic RAMs.

1.1.2 Video Monitor

The Concept video monitor is a Ball™ HD Series display unit. Under Direct Memory Access (DMA), approximately 55K of main memory is ported directly to the 720 pixel bit mapped screen. The data is transmitted to the screen at approximately 33 Mbits per second.

The 15-inch monitor is mounted to allow the swivel or tilt of the screen for maximum operator comfort. The screen can be operated in either a vertical (portrait) or horizontal (landscape) mode. Features of the monitor are:

- 15-inch CRT
- Bit mapped display
- Vertical tilt of +17 to −13 degrees
- Horizontal swivel of 90 degrees
- 720 pixels by 560 pixel screen
- 120 characters by 56 lines in the landscape mode
- 90 characters by 72 lines in the portrait mode
- Software generated character set

1.1.3 Keyboard

The compact keyboard is manufactured by Keytronics™ to Corvus specifications. Its features include:

- Selectric™ style alphanumeric keys
- Cursor movement keys
- 15-key numeric pad
- 10 programmable function keys
- Programmable character set
- Detachable coiled keyboard cable

1.1.4 Power Supply

The power supply, located in the base unit, is manufactured by AC/DC.™ The Power Supply provides:

- +5VDC at 8A (60Hz, derate 10% for 50Hz)
- +12VDC at 1.7A (60Hz, derate 10% for 50Hz)
- −12VDC at 1.7A (60Hz, derate 10% for 50Hz)

The Processor and Memory Boards consume:

- 6A at 5VDC
- 130 mA at +12VDC (RS-232C)
- 170 mA at −12VDC (RS-232C)

Available power for shared I/O slots is:

- +5VDC at 500 mA
- +12VDC at 1.5A
- −12VDC at 1.3A
- −5VDC at 200 mA

- 100/120VAC or 220/240VAC selectable
- 50Hz or 60Hz
- 200 Watts

1.2 Concept Options

Corvus Systems offers an array of options for the Concept. These include software packages, storage devices, and network capability. See the Service Manual for each hardware option for complete specifications.

1.2.1 Operating System Software

Some of the software packages provided on floppy diskettes for use with the Concept are:

- CCOS Operating System
- USCD P-System Operating System
- ISO Pascal with UCSD extensions (native code complier)
- FORTRAN 77 (native code complier)
- 68000 Assembler
- EdWord™ Wordprocessor
- Corvus LogiCalc™ Electronic Spreadsheet

A complete list of current software may be obtained from the Corvus Systems Marketing Department.

1.2.2 Floppy Disk Drive

Manufactured by Tandon™ Corporation, the 8-inch Floppy Disk Drive is available with these features:

- 250 Kbytes formatted capacity
- Single-sided, single-density IBM 3740 format
- Read and write capabilities

In addition, a 5¼ inch Read-Only Disk Drive with a capacity of 140 Kbytes may be purchased from Corvus.

1.2.3 Winchester Disk Drive Options

Mass storage is provided for the Concept by a line of Winchester Disk Drives. Interface to the Concept is through a 50-pin I/O slot on the Processor Board. The drive models are:

Rev B

- Model 6—5.7 Mbytes formatted
- Model 11—10.8 Mbytes formatted
- Model 20—19.7 Mbytes formatted

H-Series

- Model 11—12.1 Mbytes formatted
- Model 20—18.4 Mbytes formatted

1.2.4 Archival and Backup Options

Archival and backup storage can be accomplished with the Floppy Disk Drive or the Corvus Mirror® option. The Mirror is used in conjunction with a video recorder to provide a copy of a Corvus Disk Drive on video tape. For details of the Mirror, see the Mirror Service Manual.

1.2.5 Network Option

Corvus OMNINET circuitry is included on the Processor Board. The OMNINET Disk Server and related hardware feature:

- One million bit per second transfer rate
- 64 possible network devices
- Twisted pair transmission cable
- 4000-foot network length

CHAPTER 2
FUNCTIONAL DESCRIPTION

CHAPTER 2
FUNCTIONAL DESCRIPTION

2.0 Scope of Chapter

In this chapter, a functional description of the Corvus Concept is presented. The two main printed circuit assemblies of the Concept, the Processor Board and the Memory Board, will each be described.

2.1 Concept Processor Board

The Processor Board of the Concept can be divided into the following sections:

- Microprocessor
- Bus Buffers
- Memory Mapper
- ROM and static RAM
- OMNINET
- 50-Pin I/O Slots
- Data Communication Ports
- Interrupts
- Memory Arbitration
- Calendar
- Bell, Timer, and VIA
- Data Acknowledge

2.1.1 Microprocessor

The Concept is based on the Motorola MC68000 8MHz microprocessor. It has a 16-bit bidirectional data bus, a 24-bit address bus, and sixteen 32-bit internal registers. Its address lines are buffered to go to many locations. The 64-pin design eliminates the need for data and address multiplexing by giving each data and address line a separate pin.

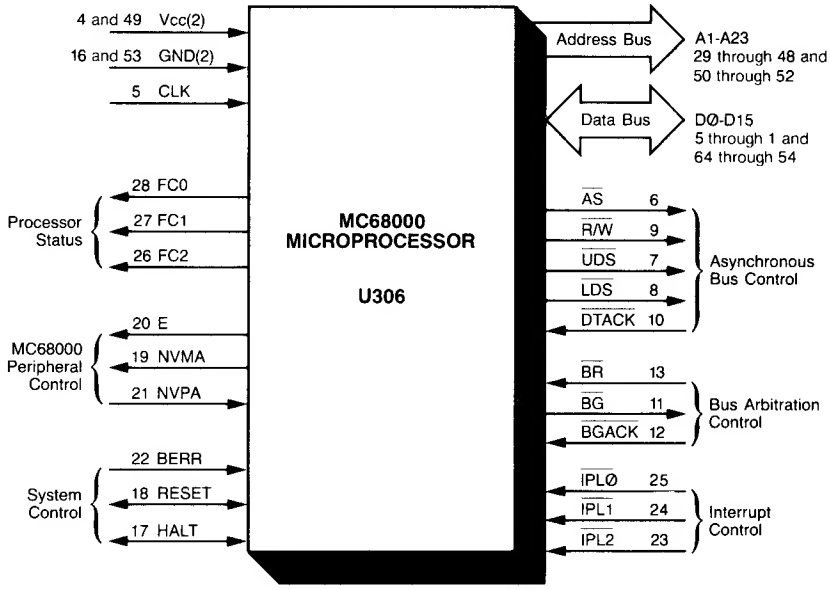


Figure 2. Motorola MC68000

2.1.2 Bus Buffers

The address bus is buffered from the processor by three 74LS244s at locations U507, U508, U407. Caution should be exercised as these buffers may be damaged if shorted together. The data bus is unbuffered to the on-board ROMs and static RAMs and is buffered to the I/O ports, OMNINET, and dynamic RAMs. If for any reason the address or data bus becomes defective the processor will assert the HALT signal and abort all operations.

The control signals (WRITE, UPPER & LOWER DATA STROBE, and ADDRESS STROBE) are buffered by a single 74LS244 at location U307. The function codes lines are decoded to determine Supervisor Mode and Interrupt Acknowledge. The Interrupt Acknowledge is connected to the Valid Peripheral Address Pin to indicate Auto Vectoring Interrupt Mode.

For further information on the processor, please refer to the Motorola 16-Bit Microprocessor User's Handbook.

2.1.3 Memory Mapper

The address space is divided into sections by a memory mapper PROM which examines the state of the address bus and selects the appropriate device.

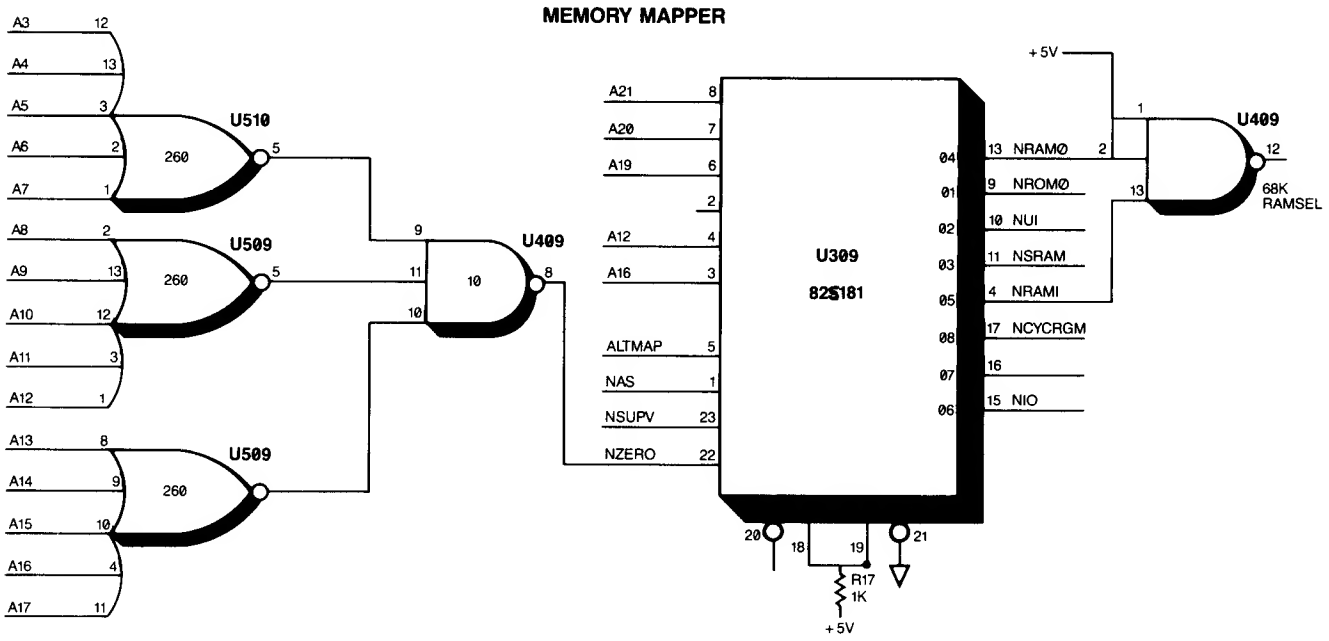


Figure 3. Memory Mapper

An 82S181 bipolar PROM examines the address lines to produce enable signals for I/O and memory. Additional inputs are NZERO, ALTMAP and NSUPERVISOR. NZERO is output from a set of gates at U309 and U510 which detect that the lower address bits are at zero. If the higher address bits are at zero and ALTMAP is zero, ROM0 will be selected for a power-on boot. If no device is selected, CYCLE ROM is asserted to prevent the processor from hanging up.

2.1.4 ROMs and Static RAM

There are four 24-pin RAM sockets and two 28-pin ROM sockets mounted on the Processor Board.

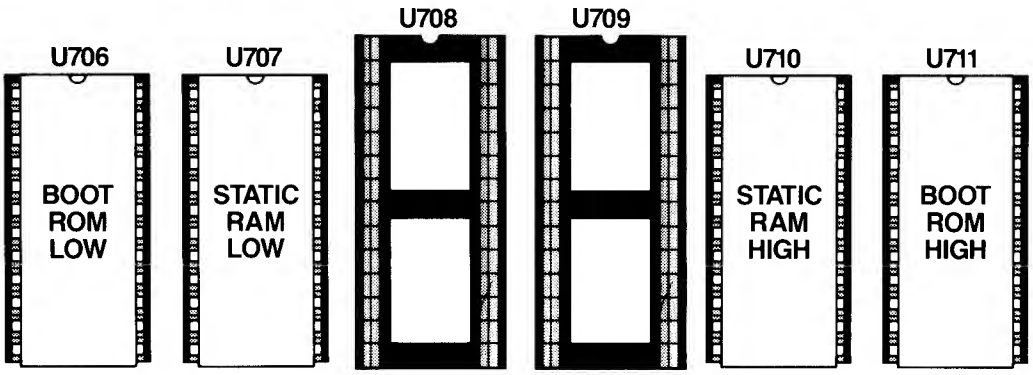


Figure 4. ROM and Static RAM Sockets

RAM sockets, locations U707 and U710, are intended to hold 2K x 8 static RAMs. These RAMs may contain system variables, jump tables, and data stored during testing. The speed of the RAM can be accounted for by jumpers K4, K5. (See Appendix H.)

The ROM0 sockets, locations U706 and U711, may hold ICs such as 2716s or 2732s. This ROM pair contains the Boot Code, initial Self Test, setup data for I/O, simple keyboard map, a character set, etc. The ROM1 sockets, locations U708 and U709, may hold such devices as 2716s, 2732s, 2764s, or other pin compatible ROMs. These ROMs may be used in loading Motorola's MACSbug for bringup and diagnostic purposes or for installing the user's firmware.

2.1.5 OMNINET

OMNINET circuitry is a self-contained unit on the Processor Board. The processor sends commands to the OMNINET transporter circuit through the I/O bus. The processor places a byte of data on the bus and strobes NOMNI. The data consists of three bytes containing an address where OMNINET is to find its command in memory. The processor checks the Versatile Interface Adapter, VIA, port A, bit 0 to see if the OMNINET is ready to receive another byte of address. OMNINET has no other connection with the processor. It talks directly to memory, preempting the processor by means of the Memory Arbiter. (See Section 2.1.9).

OMNINET'S 6801, U302, and monochip, U104, control Direct Memory Access (DMA). The Asynchronous Data Link Controller (ADLC) at U301 utilizes a pair of transmitters and receivers to balance the twisted pair cable, RS-422, for data transfer. The serial transfer rate is 1 Mbits per second. Parallel transfer by byte has a DMA rate of 125 Kbytes per second.

When OMNINET does a DMA, it takes over the address and data buses going to the Memory Board. If the MC68000 attempts to use memory during a DMA cycle it will be held off. Typically, there is a maximum one DMA cycle in 8 microseconds. During this time there can be a maximum of seven MC68000 memory accesses. DMA does not slow the MC68000 appreciably.

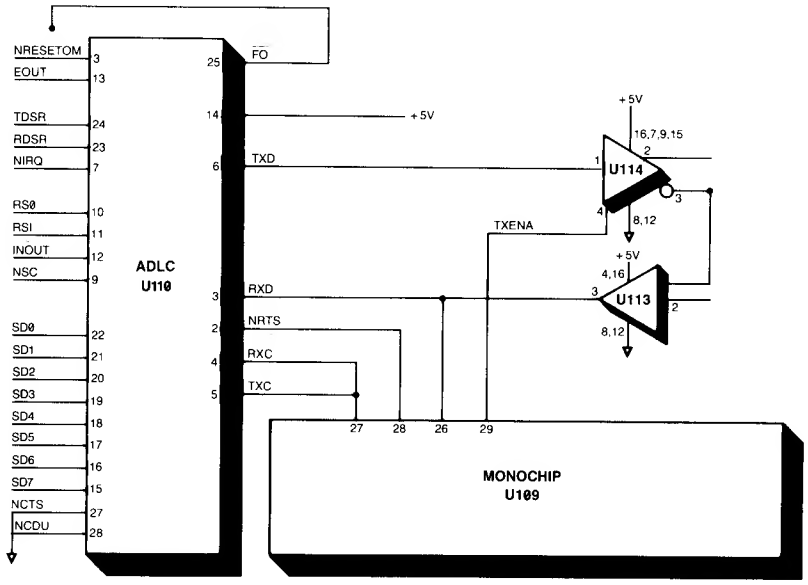


Figure 5. ADLC

To begin the DMA of a byte, the monochip asserts a DMA request, DMAREQ. This is synchronized by the Memory Arbiter which switches the memory address and data bus from the processor to OMNINET. The Arbiter begins a memory cycle and asserts DMAGO, indicating that OMNINET is in the process of doing a DMA. Following DMAGO, DMAREQ is negated. When the memory cycle is complete DMAGO is negated and the monochip sets up to accept the data into the ADLC (only on a read) and terminates the DMA cycle. Control of the memory buses are then returned to the processor.

OMNINET produces 20 address bits. Address zero is converted into upper and lower device select before being sent to RAM. OMNINET ignores address bits 21 and up.

2.1.6 50-Pin I/O Slots

Four 50-pin board edge connector slots are provided to handle other local I/O, such as to a Corvus Floppy Disk Drive or Winchester Disk System.

The I/O address space is divided into eight blocks by U605. They are subdivided as shown in Table 1.

Block 0-4	(See I/O Slots Apendix F)
Block 5	Allow reading of the NMI and IRQ lines from each of the slots on a single operation.
Block 6	Allows reading of the Clock Calendar
Block 7	Allows reading or writing to the I/O Ports. Block 7 can further be subdivided into:

0	NKBP	Keyboard	4	NCALM	Clock calendar address and Strobe register
1	NSRO	Data Comm Port 0	5	NOMNI	OMNINET Strobe
2	NVIA		6	NOMOFF	Reset OMNINET Interrupt Flip-Flop
2	NSR1	Data Comm Port 1	7	NIOSTRB	External I/O ROM Strobe
3	NVIA	Versatile Interface Adapter			

Table 1. I/O Address Space

I/O slots provide access to such devices as Corvus disk systems, parallel printers etc. These slots do not support DMA because they do not share the data and address buses with the dynamic memory. They are connected to the interrupt structure.

Table 2 gives slot pin descriptions.

Pin	Concept Signal Name	Apple II™ Equivalent	Pin	Concept Signal Name	Apple II™ Equivalent
1	NIOX	I/O SEL	26	GND	GND
2	A1	A0	27	---	DMAIN
3	A2	A1	28	---	INTIN
4	A3	A2	29	NNMI-X	NMI
5	A4	A3	30	NIRQ-X	NIRQ
6	A5	A4	31	NRESET	RES
7	A6	A5	32	---	NINH
8	A7	A6	33	−12V	−12V
9	A8	A7	34	−5V	−5V
10	A9	A8	35	---	---
11	A10	A9	36	---	7MHz
12	A11	A10	37	Q3	Q3
13	A12	A11	38	NIM	PHI 0
14	A13	A12	39	---	USER 1
15	A14	A13	40	1M	PHI 1
16	A15	A14	41	NDEVX	NDEV SLCT
17	A16	A15	42	IOD7	D7
18	NWRITE	R/W	43	IOD6	D6
19	---	---	44	IOD5	D5
20	NIOSTB	I/O STROBE	45	IOD4	D4
21	---	NRDY	46	IOD3	D3
22	---	NDMA	47	IOD2	D2
23	---	INTOUT	48	IOD1	D1
24	---	DMAOUT	49	IOD0	D0
25	+5V	+5V	50	+12V	+12V

Table 2. I/O Slot Pin Descriptions

2.1.7 Data Communication Ports

Two RS-232C ports with independent baud rates can be used for an external terminal, modem, printer, or other peripheral device. They share the I/O bus and interrupt structure with other I/O devices. The connection is by 10-wire, 25-pin sub miniature 'D' female shells, connected as Data Terminal Equipment. A modem eliminator cable is necessary to communicate with equipment other than modems.

Both serial data ports are able to communicate at baud rates from 110 to 19200, with selectable parity and word size. The receive and the transmit functions can be Interrupt generating or Non-Interrupt generating as selected.

The UART Baud Generator requires a 1.818MHz frequency which is obtained by dividing the 16.364MHz system oscillator by 9 using U212 (74LS161).

Motorola's 1488 and 1489 devices, at U213, U214, U314, and U415, transmit and receive the +12 RS-232C voltages. A 470 pF capacitor is used at each RS-232C line for speed control. The keyboard interface is driven by a Schmitt trigger inverter, U115, also used to receive keyboard data.

Three Control lines on each port are receivers: Data Set Ready (DSR), Clear to Send (CLS), and Data Carrier Detect (DCD). These can be used for handshaking or with a modem. Three Control lines Data Terminal Ready (DTR), Request To Send (RTS), and Rate Select (CH) are for output. DTR and RTS are functions of the UART, controlled by setting the UART command and control registers. CH is a bit for each port on the VIA Port B usually used for selecting between high and low speed on dual rate modems. Appendix H-2 describes the Data Communication Ports J1 and J2.

It is recommended that shielded RS-232C cables be used. If these are not available, an in-line filter is recommended. If data communication cables are strung long distances or between buildings in lightning prone areas, only Receive Data, Transmit Data, Signal Ground and Protective Ground should be used. The first three should each be connected to protective ground by a Tranzorb or other transient energy absorber.

NOTE:

There is a requirement by some European PTTs that the user be informed when a modem has gone off-line. The driver may monitor the appropriate line, transmit a message to be displayed. Also required may be logical relationships and timing between input and corresponding output control lines. As the Concept requires no hardware relationships, PTT requirements must be fulfilled by the drivers.

2.1.8 Interrupts

Six interrupt lines are served by an Auto Vectored Interrupt mechanism. The highest priority, Non-Maskable Interrupt (NMI), is not used. The two Data Com devices, the keyboard, the VIA, and OMNINET each have their own interrupt vectors. The data communication control lines shares the lowest vector with the 50-pin bus interrupt.

Although the processor can be run without interrupts, most of the I/O devices can cause interrupts so that an efficient interrupt driven operating system is created. Because 6502 I/O devices are used, which cannot produce vectors, the auto vector mode of interrupt is used. The level 7 NMI is used only when the software monitor is installed for debugging. The user cannot initiate an NMI. Interrupt Acknowledge is decoded in the following manner:

Priority Level	Signal Name	Device
7	Not Used	
6	NKEYINT	Keyboard
5	NTIMINT	VIA Timer
4	NSR0INT	RS-232C Port 0
3	NOMINT	OMNINET
2	NSR1INT	RS-232C Port 1
1	NIOCINT	Data Com/ 50-Pin Slots

Table 3. Interrupt Levels

Note that the Data Com controls and 50-pin I/O slot interrupts share the priority one interrupt. The interrupt priority can be set to any of the seven levels. An interrupt below the current level will not be served until the interrupt level is dropped to that level or below. An interrupt raises the priority level to its own level. The Return From Interrupt sets the priority to the level just prior to the interrupt. If the priority is set to 7, no interrupt can occur, thus allowing critical code sections to complete without fear of interruption. For further details, refer to the Motorola MC68000 User's Manual.

The keyboard and data communication devices are 6551 UARTS from Synertek™ Inc., Rockwell International,™ or MOS Technology.™ The Timer is part of a 6522 Versatile Interface Adapter, VIA, from the same manufacturers. Additional information about these devices can be found in the Synertek Data Catalog.

1. Keyboard Interrupts
   The keyboard UART, U310, acts as a receive only UART except during testing operations. Each time it

receives a new character, it causes a level six interrupt. Key strokes cause the keyboard software driver to send a code to the current program. Key releases cancel automatic key repeat or remove qualifies such as a shift and control.

2. Timer Interrupts
Counter U313 in the VIA is used to aid timing, including the repeat key timing. This counter interrupts every 50 microseconds with a priority level 5 interrupt. No other possible interrupt of the VIA are used.

3. Data Communication Port 0
UART U311 can be set up to interrupt on receiving or transmitting a character. It is intended for use with a terminal or modem, but can be configured for any RS-232C function. Baud rate and parity may be selected. Handshaking is covered in section 2.1.7. Each time a character is received or has been transmitted, a priority level 4 interrupt occurs.

4. Data Communication Port 1
The UART U312 is similar to that of the UART for Data Port 0. Its primary function is driving serial printers. It generates a priority level 2 interrupt.

5. OMNINET
After an operation, OMNINET generates a priority level 3 interrupt. OMNINET cannot turn the interrupt off; NOMOFF must be sent at the end of the interrupt process to turn the interrupt off (U304).

2.1.9 Memory Arbitration

The dynamic memory may be accessed by the MC68000 or an OMNINET DMA. A set of flip-flops and logic arbitrate when both the MC68000 and OMNINET try to access memory at the same time. The Memory Board requires RAMSEL before an access can start; RAMSEL must be negated before a new access can start. NRAMACK signals that the data in an access has been processed.

Signal names and their functions may be found in Chapter 5.

1. MC68000 Memory Access Without DMA Conflict
When the MC68000 produces an address in the dynamic memory range, 68K RAMSEL is asserted. It is then presented to the J input of JK flip-flop U204-11. After the Address Select (NAS) is asserted, the Q of the JK flip-flop U204-9 will become true at the next 16M clock. The Q (68KGO) is passed through OR Gate U203-8 to become RAMSEL. When the data has been processed by the memory, NRAMACK is asserted. NRAMACK then goes through an OR gate to become NTACK U203-11, and finally through the data acknowledge timing gates U411 and U510 to become NDTACK. After receiving NDTACK the MC68000 disasserts NAS, clearing the JK flip-flop and preparing for the next memory access.

2. DMA Without MC68000 Conflict
OMNINET asserts DMAREQ (DMA request) which is applied to the J of the JK flip-flop U104-3. At the next 16M clock the JK flip-flop asserts DMAEN (DMA enable) U104-5. One 16M clock time later NDMAGO U204-6 is asserted which sets DMAGO2 U104-9. NDMAGO tells OMNINET that the requested DMA cycle has begun, DMAGO2 U104-9 switches the memory address and data buses to OMNINET.

   DMAGO is passed through OR gate U203-10 to assert RAMSEL. The assertion of DMAGO causes OMNINET to disassert DMAREQ. When NRAMACK is asserted it clears DMAEN and DMAGO, causing OMNINET to accept the data (if a read was in progress) and to complete the DMA cycle. DMAGO2 follows DMAGO one 16M clock later, switching the memory and data buses back to the MC68000. The disassertion of DMAGO removes RAMACK, preparing for the next memory cycle.

3. Collisions
If a MC68000 RAMSEL occurs when DMAEN or DMAGO is true, gate U205-6 will prevent 68KGO from occurring. When both DMAEN and DMAGO2 have been disasserted, the next 16M clock will cause 68KGO to be asserted and a memory cycle to begin as before.

   If DMAEN is asserted while 68KGO is true, DMAGO will not be allowed to set. Moreover when NRAMACK is asserted it will clear DMAEN. After 68KGO is disasserted, the next 16M clock will allow DMAEN to set, beginning a DMA access now that the conflict has been removed.

2.1.10 Calendar

A battery backed up calendar is provided, to clock the time and date from tenths of seconds through months. Although leap year can be set to allow February to have 29 days, the calendar does not contain a years register. The battery may be an on-board lithium or a tray-mounted NICAD. The calendar, is very similar to a watch circuit. To read or write to the calendar, an address must be written to NCALM (calendar mode), followed by an address with a strobe written to NCALM. Next, the read or write is asserted by the signal NCALRW (calendar read/write). Finally, a zero address with no strobe is written to NCALM.

2.1.11 Bell, Timer, and VIA

The bell is a transistor driven speaker, which is driven by the shift register in the Versatile Interface Adapter (VIA). The shift register rate is determined by one of the VIA timers and the waveform of the data loaded into the shift register. The duration, pitch and timbre of the bell are determined by the bell driver and user program.

The other VIA timer is used as a system resource. Its basic function is to perform the key wait and repeat timing. When a character key is pressed its code is used; after a wait of one half a second, the code is repeated at the rate of five times per second. If the FAST key is pressed together with any character key, that character code is immediately repeated at 15 times per second.

Three VIA inputs not so far mentioned are the two boot switches and the screen orientation switch. These are read on VIA port B bits 6, 7, and 3. The boot switches indicate whether OMNINET, a local hard disk, or floppy drive is to be used as the boot device. The orientation switch is needed to indicate whether the screen is to be used horizontally or vertically. Three outputs from the VIA are VIDOFF, VA17, VA18. VIDOFF must be zero to turn the display on. VA17 and VA18 are normally zero for display. If they are not zeroed, then other than normal areas of memory are displayed.

2.1.12 Data Acknowledge

The 68000 is an asynchronous machine for memory and I/O. It asserts a memory request (derived from DATA STROBE and ADDRESS STROBE) and waits for memory acknowledge (DTACK). Memories and I/Os of different speeds are accommodated by delaying data acknowledge (DTACK) until the access is complete. In the Concept the DTACK is provided by either a state machine (dynamic RAM I/O or by the combination of the device select ROM). DTACK is provided by either a state machine (dynamic RAM, I/O) or by the combination of the device select (ROM, static RAM) and a delay. The circuitry that is involved consist of U411, U511 and U510. The delay is from a shift register (U412). The shift register clocks in ones unless cleared by DATA STROBE being negated. It has outputs at intervals of 61 nsec up to about 490 nsec which can be selected by a jumper for each of the ROM and RAM pairs. This allows for access times of zero to about 600 nsec to be used. The delay from the state machines varies by up to a microsecond (dynamic RAM) or up to 2 microseconds (I/O). Gates U411, U510 and U511 form the delayed signal into NDTACK (TP 20) Data Strobe DS can be seen at TP 19 and Not Address Strobe at TP 11. If the MC68000 encounters illegal conditions (e.g. instructions), it will halt with a low at TP 14.

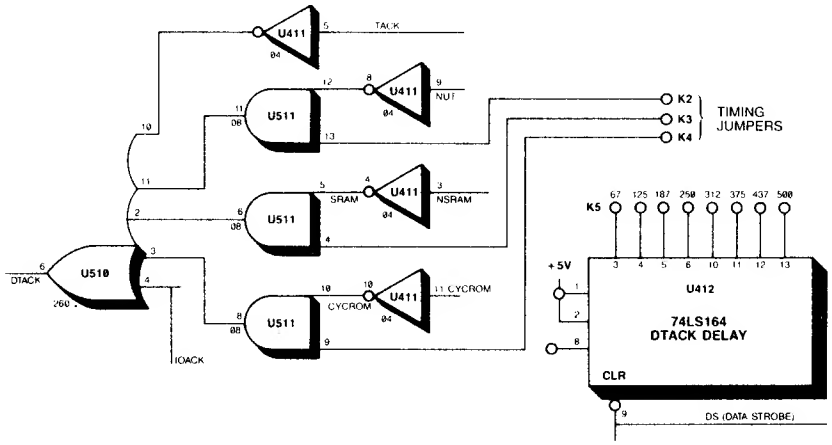


Figure 6. Data Acknowledge Timing

2.2 Concept Memory Board

The Memory Board provides most of the read/write memory for the system. It functions in eight categories:

- Horizontal Timing
- Vertical Timing
- RAM Timing
- Memory Selection
- Address Multiplexing
- Memory Array
- Memory Buffer
- Video Shift Registers and Multiplexer

The horizontal counter produces high speed timing for the system, including horizontal synchronization and blanking pulses for the video monitor. Similarly, the vertical counter produces vertical synchronization and blanking pulses. RAM timing includes Row Address Select (RAS), Column Address Select (CAS), and Multiplexer Address (MUX) times for the memory array. The video address counter provides both screen and memory refresh. Data from the memory array is read into the memory buffers and then to the processor. It may also be read to OMNINET or to the video shift registers and from there to the screen.

2.2.1 Oscillator

The oscillator is a self-contained crystal oscillator with a frequency of 16.364MHz. This frequency is used as the base frequency and is divided to fit system needs.

2.2.2 Horizontal Timing

A 16.364 MHz oscillator is counted by 2, 16 and 512 to produce signals of approximately 8 MHz, 1MHz and 32 KHz. 32 KHz is the horizontal scanning frequency of the monitor. The Processor Board uses the 16MHz, 8MHz and 1MHz signals to clock various devices. The horizontal timing section is comprised of an oscillator, three counters, a logic array, and flip-flops for resynchronization of signals.

Not Horizontal Blank Previous (NHBLANKP) is clocked into the 74LS174 to produce the horizontal blanking signal NHBLANK. Note that N suffixed to a signal means that the signal is asserted when it has a low voltage.

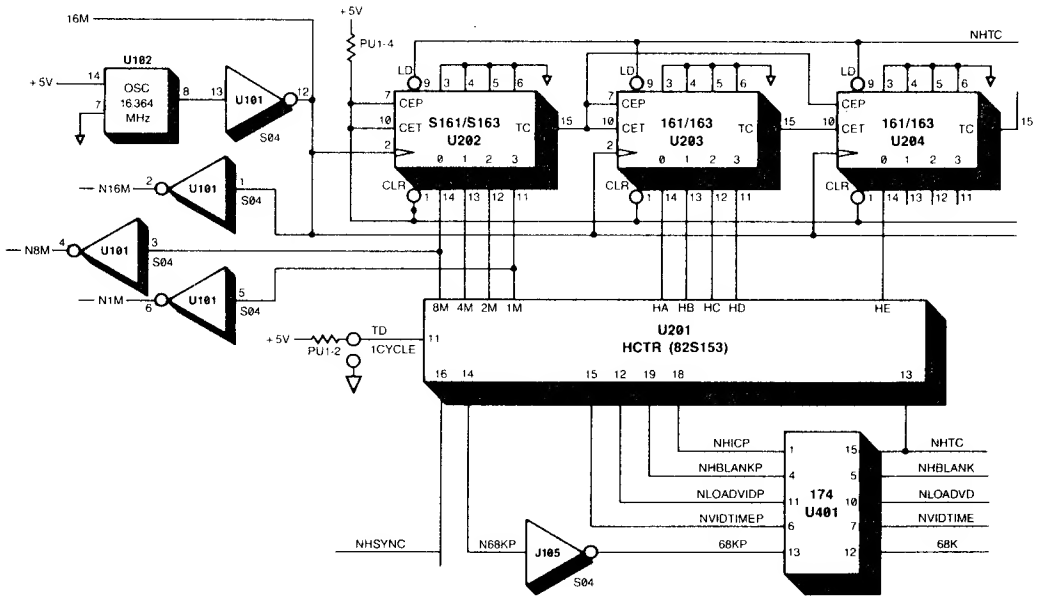


Figure 7. Horizontal Timing Circuit

The memory fetches data for the video shift registers during video-time and can read or write data for the MC68000 or OMNINET during non-video-time. NVIDTIMEP is clocked into the 74LS174 to produce the signal NVIDTIME, as are NLOADVIDP previous and 68K Previous. NLOADVID instructs the video shift registers to load the data from their data lines. 68K allows the memory to start a read or write cycle for the processor. Its timing is so chosen that a memory access will finish before the next video-time. At the video-time a memory access will start and will be complete by the next 68K-time. 1 CYCLE allows one video-time to be between each 68K-time. If 1 CYCLE is not true there will be one video cycle to every three 68K-times. Also during horizontal blank time there will be continuous 68K times and no video times. The 68K time is an enable signal: the memory makes an access when a 68K signal and a MC68000 read or write request coincide. NHSYNC provides the horizontal synchronization for the monitor.

2.2.3 Vertical Timing

The vertical timing counter is comprised of similar devices to the horizontal counter. It produces the Vertical Synchronization (VSYNC) signal for the monitor, and vertical blanking (VBLANK) signal which it combines with the horizontal blank signal to enable video to the monitor. The vertical timing counter is clocked by NHBLANK and resets itself at 60Hz unless the 60Hz jumper is grounded which causes a 50Hz rate to be used. (See Appendix G). A signal HOME clears the video address counter so that every screen begins to refresh its data at the same point.

2.2.4 RAM Timing

The Row Address Select (RAS), Column Address Select (CAS) and multiplexing signal are produced by a 74S195 shift register. Input logic allows either video time or the MC68000 to initiate a memory cycle. As soon as RAS time is asserted (NRASTIME is low) feedback keeps the input low until the CASTIME signal, delayed twice through a 74LS174, puts the 74S195 in the "load" condition. Logic high signals are loaded for three clock times assuring that the RAM precharge times are fulfilled.

A 74LS74 flip-flop pair, U403, controls MC68000 access to the memory. The first flip-flop sets following a MC68000 memory request (RAMSEL) and the 68K signal. A memory cycle occurs until NCAS goes high, setting the second flip-flop and asserting Data Acknowledge (NRAMACK). Eventually MC68000 will disassert RAMSEL, resetting these two flip-flops. Only when the first flip-flop is set and the second not set, is a read or a write permitted to the MC68000.

2.2.5 Memory Selection

The Bank Selects and RAS, CAS, and WRITE signals are generated by 74LS139, 74LS08 and 74LS32 devices. A RAS occurs on all banks together during video-time but only on one bank at a time for the MC68000. The MC68000 may read the upper, lower or both sections of the bank in a memory access.

2.2.6 Video Address Counter

This counter sequentially addresses all locations of memory displayed on the monitor, including some overlap during horizontal and vertical retrace. The counter increments during horizontal display but does not increment for most of horizontal blank. The memory accesses two banks at a time, causing the counter to be incremented by two each video time. If four banks of memory are installed, all four banks of data are loaded into the shift registers at once, clearing the memory. Jumper TJ is then set to increment the counter by four. (See Appendix G)

2.2.7 Memory Multiplexing

During video time, the video address counter is selected to address the memory, otherwise the MC68000 or OMNINET addresses the memory. The signal NMUX determines whether the lower or upper part of the address goes to the memory to be strobed by RAS or CAS. Only the lower part of the video counter is necessary to refresh the memory, but all of the counter is necessary to refresh the screen. Jumpers allow selection correctly when two or four memory banks are installed. (See Appendix G)

2.2.8 Memory Array

The memory is divided into 4 banks of 16 (64K) RAMS each. The banks are in turn divided into upper and lower bytes of 8 (64K) RAMS each. For full video to occur at least two banks must be installed.

2.2.9 Memory Buffers

The data from the memory is latched into buffers at the end of each 68K memory cycle. Data can be read from the buffers if the MC68000 is requesting a read. If the MC68000 is not reading, the buffers are tristate.

2.2.10 Video Shift Registers

The video data stream requires a data rate of 32 MHz. To achieve this 32 bits (two words) are loaded from 2 banks each microsecond (or four words alternate microseconds if four banks are installed). The shift register is clocked at 16MHz but is split in two. Bits are taken alternately from each half during a clock cycle, thus doubling the data rate.

CHAPTER 3
DISASSEMBLY

CHAPTER 3
DISASSEMBLY

3.0 Scope of Section

The chapter describes the initial inspection and disassembly of the Corvus Concept. It is very important to perform the visual inspection described in Section 3.2 to insure that the Concept was not damaged during shipment and that the order is complete. Additional installation instructions for peripheral equipment may be found in the appropriate Installation or Service Manual.

3.1 Installation

See the Corvus Concept Workstation Installation Guide for installation instructions.

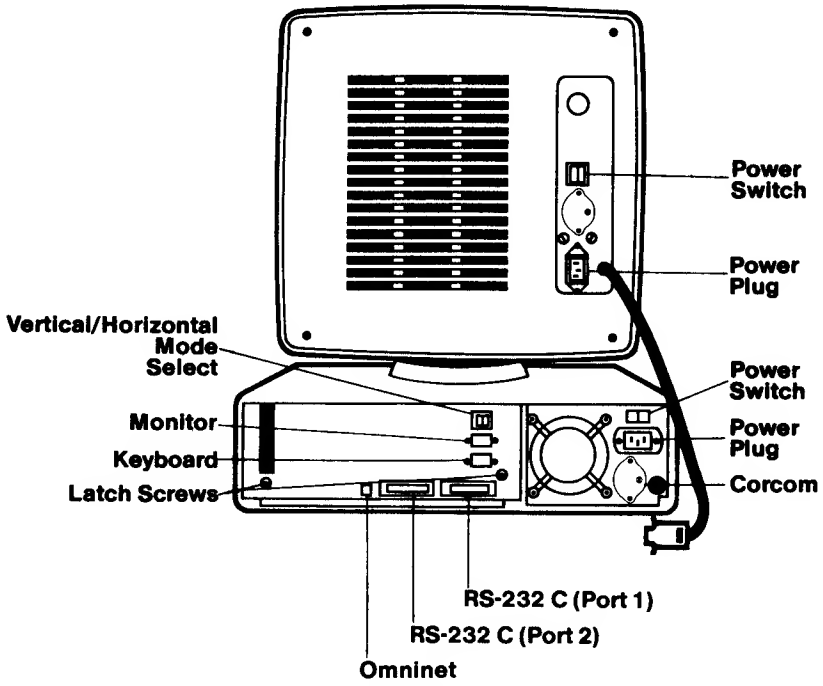


Figure 8. Concept Rear View

3.2 Visual Inspection

Any time a Concept is received, several checks should be performed before the Concept is installed at the customer site. Each Concept should be carefully unpacked and checked for shipping damage. External evidence of rough handling may be symptomatic of damage within the Concept.

NOTE:

Any damage claims must be reported to the local office of the shipper so an inspection may be made, and a damage report filed. Also, if the damaged equipment is a new product, the Corvus Order Processing Department must be contacted for proper return procedures. If the damaged equipment is a recently serviced product being returned under an RMA number (Return Merchandise Authorization number), contact the Corvus Customer Service for proper return procedures.

3.3 Video Monitor Removal and Disassembly

1. Turn the power off and remove the cables from the monitor to the base unit.
2. Remove the monitor unit from its base by pressing in the latch under the front of the monitor and carefully lifting the front of the monitor up and sliding it back.
3. Facing the front of the monitor, grasp opposite corners of the front bezel and pull carefully.
4. With the bezel off, remove the four allen head screws that hold the monitor in the cabinet. Remove the monitor from the cabinet.

3.4 Keyboard Disassembly and Cleaning

The Keytronics keyboard is a complete module. If the keyboard becomes defective the entire unit should be replaced. The keyboard may become dirty causing sticky keys or poor contacts. Remove the four screws holding the keyboard within the base. The dirt inside can be blown out with dry air. The external cable should be checked for continuity.

3.5 Electronics Tray Disassembly and Assembly

The following procedures should be followed to remove the electronics tray from the Concept base.

1. Turn the power switches off on the base unit, video monitor, and peripheral equipment.
2. Remove all cables from the back of the base. This includes the cable from the monitor, from the keyboard, tap cable if OMNINET is being used, and the power cord. Cables to interface cards within the Concept base should be removed when the tray has been opened.
3. There are two latch screws on the back of the tray. Loosen these screws by turning the left one, as you face the back, clockwise. The latch screw on the right should be turned counterclockwise. The tray may now be pulled partially out. See Figure 9 for latch screws and cable locations.

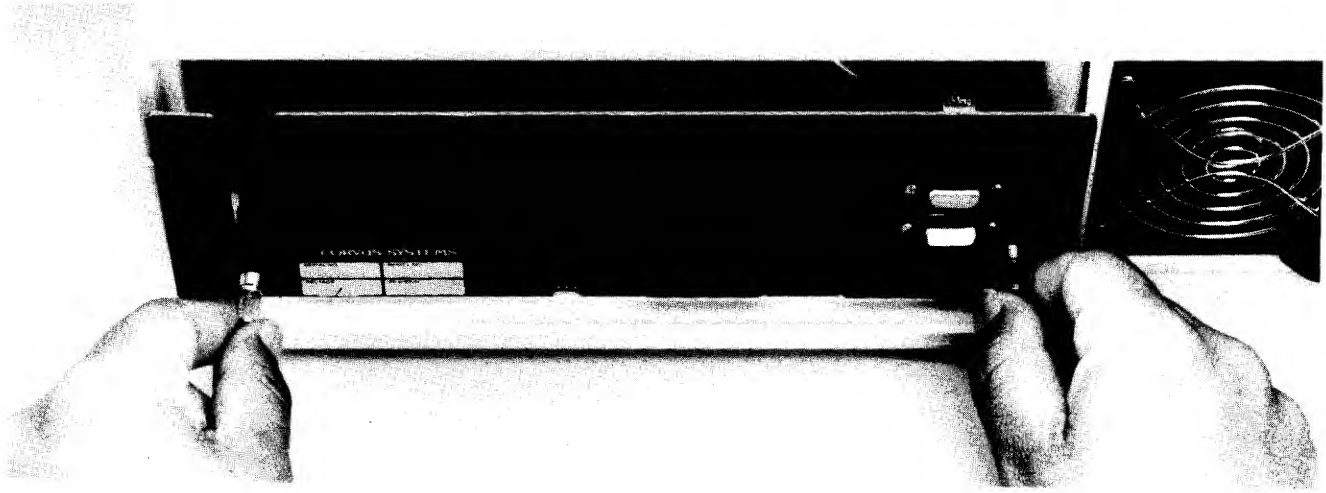


Figure 9. Latch Screws

4. To completely remove the tray, the four wire DC power cable from the Processor Board and the two wire cable from the Memory Board must be disconnected.

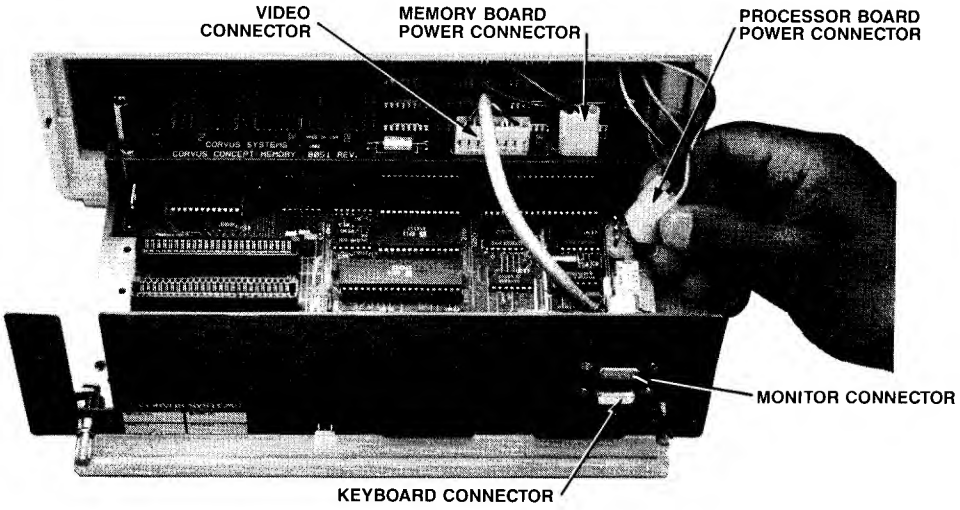


Figure 10. Electronics Tray Power Connections

5. Pull the tray out of the base cavity. If resistance is encountered, lift slightly as you pull.
6. Disconnect the speaker wire leading to the Processor Board. Remove the four allen screws securing the speaker tray. Remove the Speaker Tray.
7. Disconnect the cable from the Memory Board. Remove the stand-offs that support the speaker tray. Remove the three flat ribbon cables at connectors J4, J5, and J6. Lift out the Memory Board.
8. Remove the four stand-offs that supported the Memory Board. Disconnect the keyboard and power switch connector at J9. (See Appendix A-3.) Remove the remaining allen screws which secure the Processor Board. To access the allen screws at the back of the tray, unscrew the retainer nuts on the latch screws. Lift out the Processor Board taking care to disengage the two serial ports from the back panel of the tray.
9. Reassemble the tray following the above steps in reverse order. Cables should be routed under the speaker tray to prevent interference when replacing the electronics tray.

3.6 Power Supply Removal

1. Follow Electronic tray removal steps 1-5.
2. Carefully remove the video monitor from the base following instructions in Section 3.3.
3. Turn the base unit on its side and remove the five allen screws from the bottom of the base.
4. The top cover should now be free to remove revealing the open and exposed power supply.
5. Remove the four allen screws securing the power supply to the base.
6. Disconnect the muffin fan. Separate the six wire connector leading from the power supply to the CORCOM wire harness.
7. Remove the power supply from the base.

CHAPTER 4
ADJUSTMENTS

CHAPTER 4
ADJUSTMENTS

4.0 Scope of Chapter

This chapter will guide you through the necessary steps to adjust the power supply and align the video monitor. Transportation and handling may necessitate these procedures.

4.1 Concept Power Supply Adjustments

The tools needed for the adjustment of the power supply are:

- Digital voltmeter
- Alignment tool or small screwdriver

1. Follow the Power Supply Removal and Disassembly procedures in steps 1 through 4 of section 3.6.

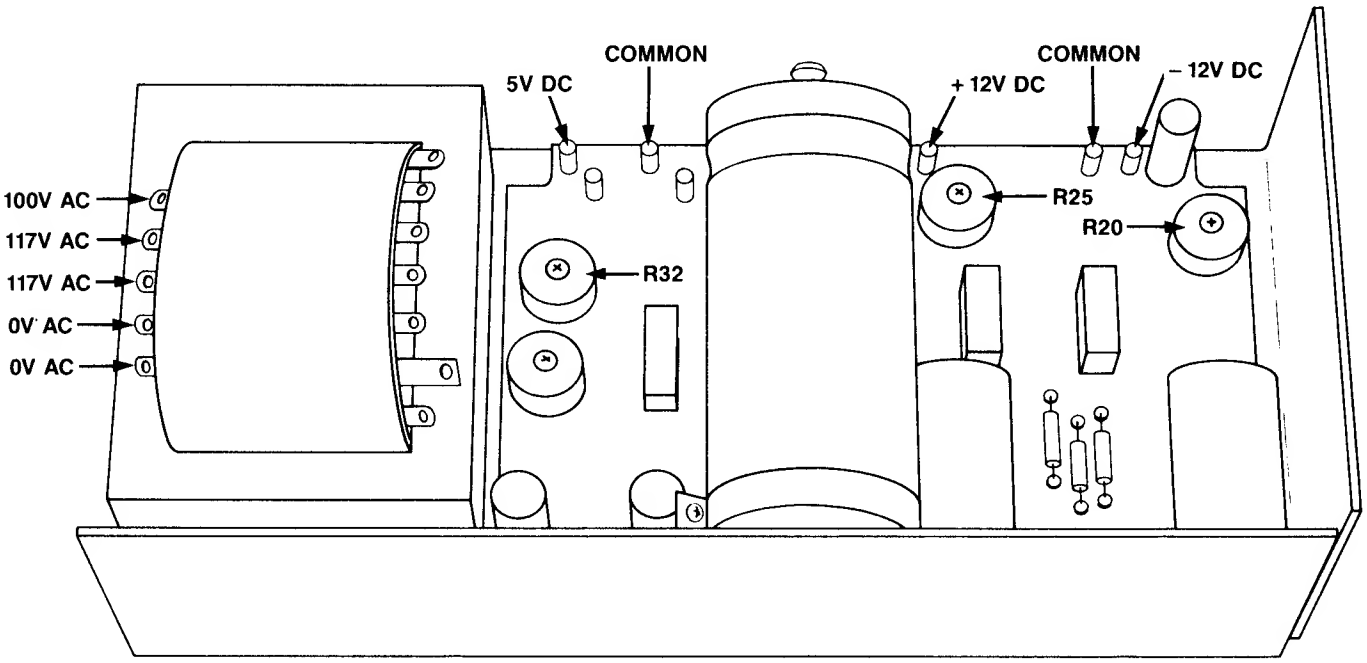


Figure 11. Concept Power Supply Test Points and Adjustments

2. While measuring the output at one of the Test Points, insert an alignment tool into the associated trim pot. Adjust to within the tolerance ±0.10 V.

   - R32 for +5VDC
   - R25 for +12VDC
   - R28 for −12VDC

   If the power supply cannot be adjusted to within tolerance, contact Corvus Customer Service.

4.2 Preparations for Video Adjustments

Tools that are required for a video adjustment are:

- CRT alignment tools
- Plastic see-through ruler
- Jumper with clip leads

1. Using a non-indelible marker, lightly trace the inner parameter of the front monitor bezel onto the screen of the CRT. This will aid when centering the raster and setting the proper vertical and horizontal lengths.
2. Perform the disassembly procedures in Section 3.3, position the exposed monitor on the base unit in the horizontal (landscape) position. Connect the monitor. Set the Screen Orientation Switch for horizontal display.

4.3 Video Alignment and Adjustment

Some adjustments may not be required; others may need to be performed more than once. All adjustments should be done in the horizontal mode and repeated in the vertical mode. It may be necesary to re-check adjustments in the horizontal mode.

WARNING:

To prevent possible shocks it is recommended that you use one hand only when adjusting video equipment. Keep the other hand away from all equipment, preferably in a pocket.

1. Apply power to the system allowing a minimum of 10 minutes for the monitor to warm-up and stabilize.
2. Log-on to the Concept.
3. When the Function Key labels are displayed, select the Window Manager function by holding down the command key and pressing function key F2 simultaneously. A new set of Function Key labels will appear.
4. Select the TestPtrn function key by holding down the command key and pressing Function Key F9 simultaneously. The screen will prompt the user to select a grid pattern or a pattern of pixels. A grid will be used for vertical and horizontal adjustments; pixels will be used for focusing and brightness adjustments.
5. Raster Centering
   Turn the Brightness knob on the rear of the monitor to maximum. Using the two metal tabs on the yoke of the CRT, (see Figure 12) move the raster until it is centered horizontally within the lines made in Step 1 of Section 4.2.

   If the raster is not parallel to the sides of the display glass, the yoke must be rotated. To rotate the yoke, slightly loosen the clamp screw on the neck of the CRT. Grasp the yoke assembly and gently rotate until the raster is properly oriented. DO NOT slide the yoke forward or backwards as this will affect horizontal linearity. Tighten the clamp screw.

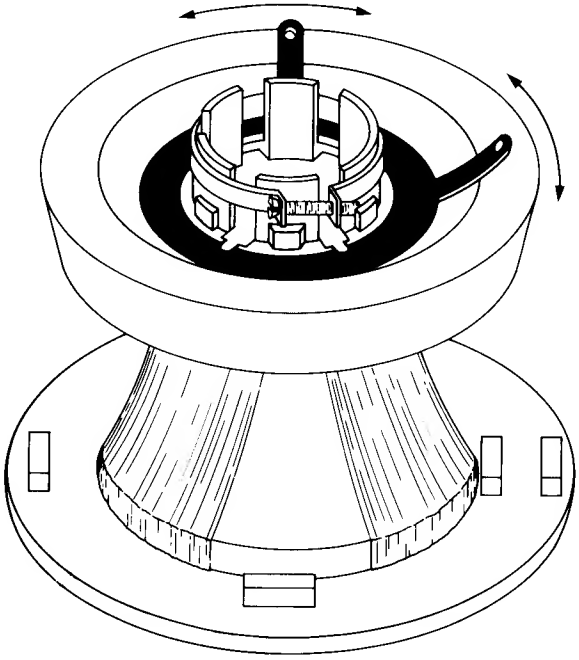


Figure 12. CRT Adjustment Yoke

6. Horizontal Data Centering
   Select a grid pattern of 4 or 8. Turn the H. DATA CENT trim pot R111 (see Figure 13) until the grid is centered within the raster. A poorly aligned screen may exhibit fold-over.

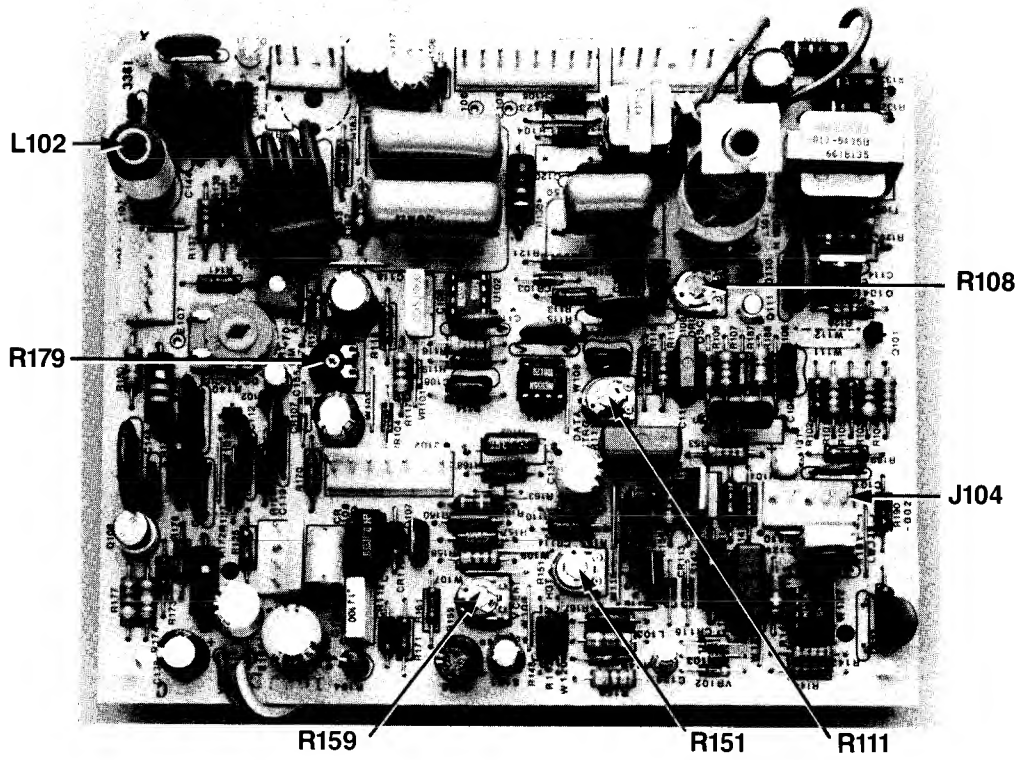


Figure 13. Horizontal and Vertical PCA

7. Vertical Height
The vertical dimension of the grid, the shorter side in the landscape mode, should be 7.75 inches (19 centimeters). Measure the center line with a clear plastic ruler. Turn the Vertical Height trim pot R151 (see Figure 13) until the proper dimension is achieved.

8. Vertical Centering
Adjust the Vertical Centering trim pot R159 (see Figure 13) to center the display on the screen. It may be necessary to readjust the vertical height.

8. Horizontal Width
Ensure that the grid is centered. Using a plastic trim tool adjust L101 (see Figure 13) until the horizontal width measures 10.5 inches (27 centimeters). Use the center line of the grid for measurements. It may be necessary to repeat Steps 5 and 6.

9. Brightness
Turn the Brightness Limit trim pot R179 (see Figure 13) until the raster is just visible. Turn the Brightness knob on the rear of the monitor through the entire range. The display should go from fully dark to a data display with the raster just visible.

10. Contrast
Adjust the trim pot on the Video Board (see Figure 14) until the image begins to smear. Back up the adjustment until the image is clear and stable.

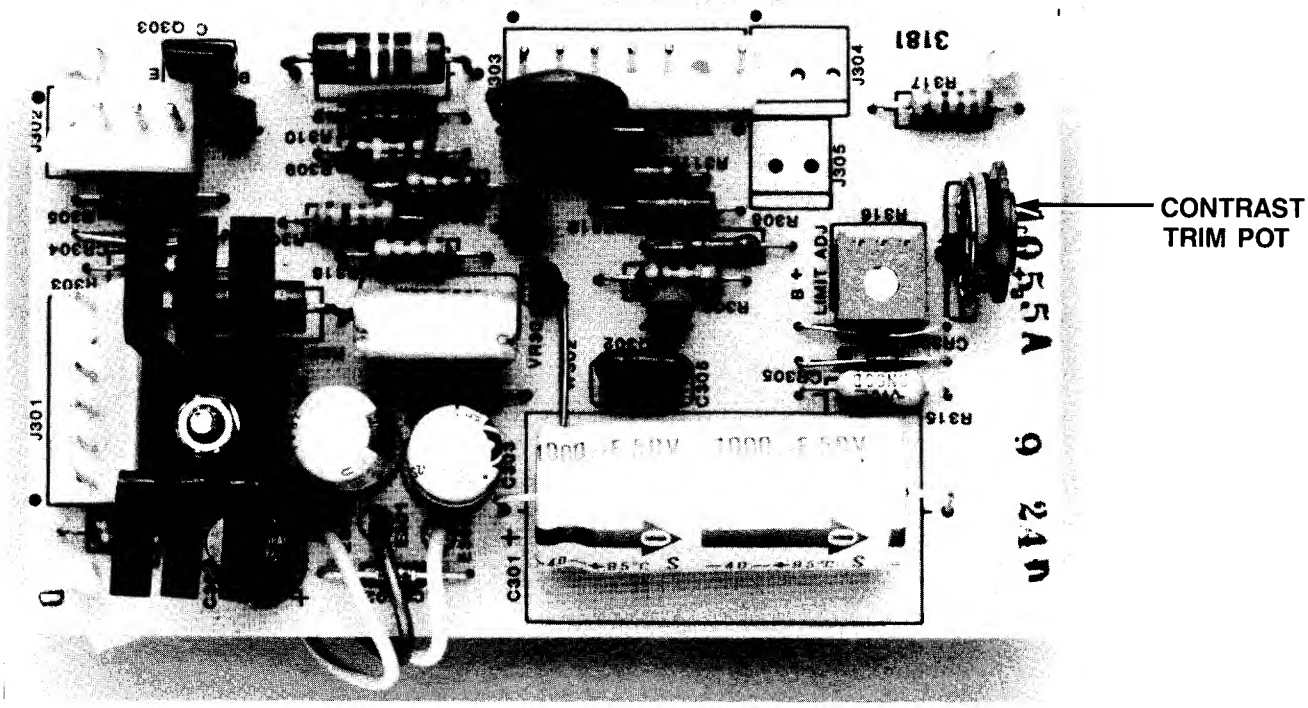


Figure 14. Video PCA

11. Horizontal Oscillator
    Using a shorting clip, connect J104 to the junction of C101 and R103. This allows the oscillator to run free. Turn the Horizontal Oscillator trim pot R108 until the display is stable and readable. Remove the clip and cycle the power to the monitor two or three times to insure that the oscillator will lock at the proper frequency. If the display is no longer centered, repeat Step 1.

12. Final Display Position
    Turn the monitor to the portrait mode, vertical. The leftmost line should be parallel to the edge of the metal frame around the CRT and at a distance of 2.375 to 2.5 inches (6 to 6.4 centimeters). If the line is parallel but the distance is incorrect, readjust the Vertical Centering trim pot. If the grid is centered but the leftmost line is not parallel, the CRT must be rotated inside the frame.

13. Focus
    To adjust the focus select a pixel pattern. With the raster just visible, the dots in the center of the screen should be clear and sharp with no tails or smearing when viewed from a distance of six feet (1.75 meters). The outer portions of the display may show slight tails, but they should not extend to the next dot. DC FOCUS, R140, and H FOCUS, L102 are used for adjustment.

CHAPTER 5
TROUBLESHOOTING

CHAPTER 5
TROUBLESHOOTING

5.0 Scope of Chapter

The Corvus Concept's modular design makes on-site, Level 1, troubleshooting fast and efficient. Level 1 troubleshooting includes initial checks and procedures to isolate defective modules. Boot problems and Self Test failures are described as are solutions.

Once the problem module has been identified, further troubleshooting may be necessary to diagnose defective modules. Level 2 troubleshooting procedures are intended for trained servicing dealers. Diagnostics are accomplished through utilization of modified Motorola MACSbug™ routines.

This chapter describes both Level 1 and Level 2 procedures, and Test Points and their associated signals.

5.1 Level 1 Troubleshooting

When making an on-site diagnosis, a complete spare parts kit is required.

The first step in troubleshooting is to duplicate the problem. Due to many variables such as setup, initialization procedures, software, external devices, and the environment, the problem may not repeat on a consistent basis.

Once the problem is noted, the second step is to isolate the failure by a process of elimination. Begin by eliminating sections of the system that are not required to repeat the failure. For example: If the monitor has no raster, it would be safe to eliminate the floppy drive from the system. Note that if the symptoms disappear after removing a certain section, that section may be the problem area. Do not remove peripherals needed to run the diagnostic tests.

The third step is to substitute a suspect module with a known good module. If the problem disappears, reinstall the suspect module to see if the problem returns.

CAUTION:

If the suspect module is burnt, discolored, or extremely hot to touch, do not substitute with a known good module. There is a risk that something external to that module caused the damage.

5.1.1 Video Monitor

The video monitor is a BALL HD series. In case of failure, the monitor unit should be returned for repair or replacement. In all cases where a malfunction of the monitor is suspected, the following guidelines should be followed prior to returning the monitor:

1. Ensure that proper signals are being sent from the video controller by substituting a known good base unit. If the monitor still does not work try the following checks.
2. Ensure that the proper AC line voltage is applied to the monitor (110 VAC, 120 VAC, 220 VAC, or 240 VAC). By loosening the left screw, the CORCOM can be adjusted to match the line voltage used in your area. (See Figure 14.) Ensure that the fuse link is good by checking for continuity.

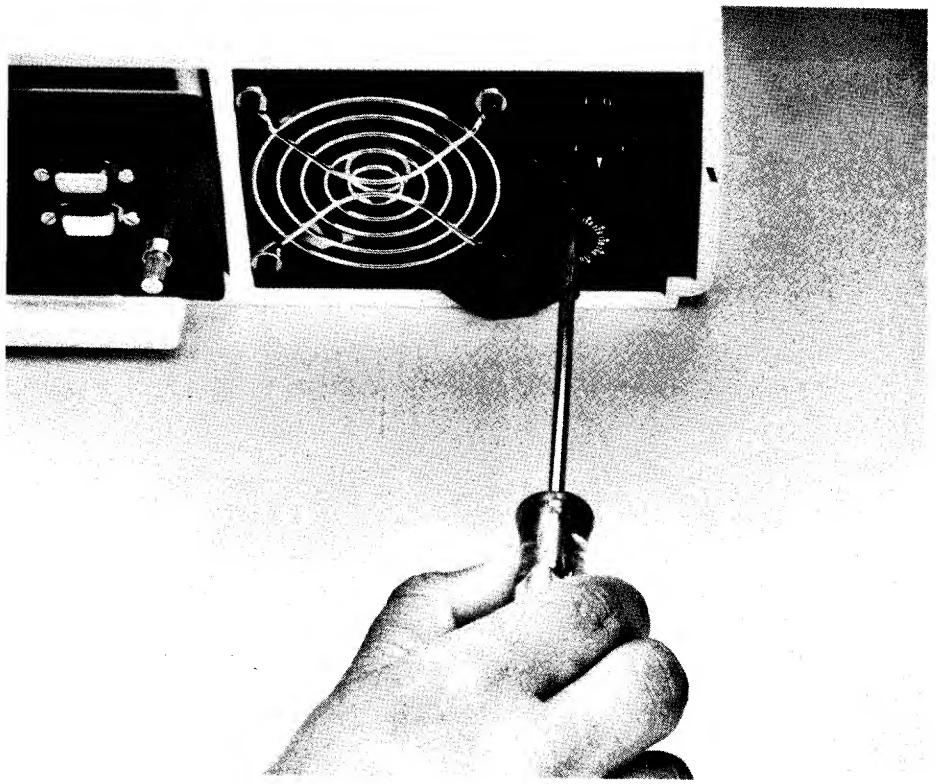


Figure 15. CORCOM Setting

3. Check the seating of internal plugs and connectors. During shipment they may work loose.
4. Remove the four screws that hold the back panel in place. Locate the low voltage PCA at the bottom of the unit. Check for proper voltage at Test Points 301 and 302. (See Figure 16.)

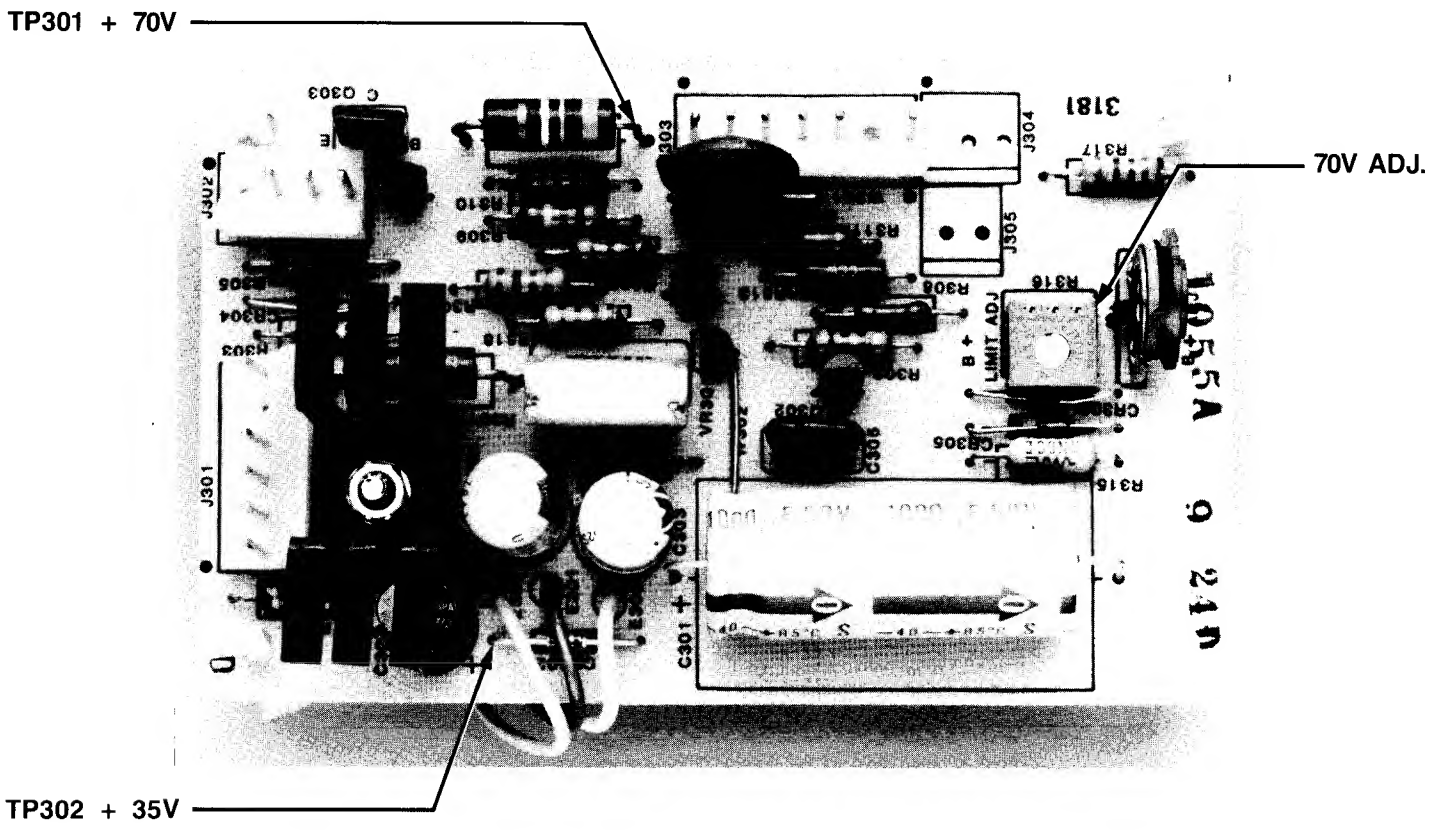


Figure 16. Monitor Voltage Test Points

5. Check the brightness and contrast levels by adjusting both controls through their entire range. Refer to the Video Alignment section.

5.1.2 Power Supply

The power supply cannot be physically eliminated from the unit. Therefore it must be checked first to verify that it is not the cause of the problem. See Section 3.6 for Disassembly and Section 4.1 for Adjustments.

1. If the DC voltages are not present, check to see if the muffin fan is turning. This indicates that the line voltage is present. If the fan does not turn, check the primary windings of the transformer with an AC voltmeter. (See Figure 11.) This voltage should be equal to the line voltage.
2. If there is no primary voltage, check the fuse link. If the fuse link is good, check the continuity of the on/off switch and ensure that the power cable is inserted snugly into the CORCOM.
3. If the voltages are incorrect, check the voltage select on the back of the unit. (See Figure 15.) Insert a slotted screwdriver into the selector and turn to the proper line voltage.

4. With a DC voltage meter measure the voltages at the I/O slots. Measure the following pins of any 50-pin I/O slot:

   - Pin 25 / +5V
   - Pin 26 / GND
   - Pin 33 / −12V
   - Pin 34 / −5V
   - Pin 50 / +12V

   If any of the voltages varies more than ± 5%, adjust it to the proper voltage. If voltages cannot be adjusted, replace the power supply.

5.1.3 Power-On Self Tests

On initial power-up the Concept can self diagnose a hardware failure. The initial Self Test will verify that both data communication UARTs and the keyboard UART are in working condition. The Self Test will verify boot PROM checksums, will read and write several patterns to static RAM and dynamic RAM, interrogate the I/O slots for known devices, and will check for OMNINET duplicate host numbers.

A 555 timer operates so that the NRESET, NRESETOM, and HALT signals are held low for several clock times, resetting hardware and causing the MC68000 to begin addressing location zero, which is the first word of ROM0. The first two words are zero and set up the supervisor stack pointer and program counter. The second two words are the address of the fourth word of ROM0, to which the program counter is set. The next instruction sets the status register to 7 so that only the Non-Maskable Interrupt (NMI) can cause an interrupt. Since NMI is connected only during manufacturing, no interrupt should occur for a user. The program continues with a brief Self Test.

All on-board I/O registers are exercised. If there is an error, the Concept will attempt to inform the user by beeping the speaker, filling memory with a checkerboard pattern, displaying "bus error" and sending "bell" characters on Data Com ports. A serious problem may prevent some or all of these actions. If there is no error, the processor will perform a checksum on the ROM, and write and verify an incrementing pattern in the static RAM. If these tests are successful system variables are written into the static RAM.

Next the UARTS baud rates, parity etc., are set up to default conditions: 9600 baud for the Port 0 UART, 300 baud for the Port 1 UART, and 600 baud for the keyboard UART. The shift register and counter are set up to give a beep and the OMNINET interrupt is cleared.

The address of the first word of every 256th location is written into dynamic RAM for the first one megabyte of that memory, and then read back. The first bank must return the correct value when read. Incorrect values from the third and fourth bank will cause the system to assume that those banks were not loaded. Next, an incrementing pattern is written across all dynamic RAM and verified; the pattern increments by one byte with an extra increment each 256 locations. If this test is successful, zeros are written throughout the RAM, the display is turned on (0-VIDOFF), and a boot message appears. If the boot switches on the Processor Board are set for a choice of booting device (see Figure 17 and 18 for switch settings), the following message will appear:

```
CORVUS Concept INITIALIZATION (0.4)
©COPYRIGHT 1982 CORVUS SYSTEMS, INC.
ALL SYSTEMS PASSED
SELECT (D,F,L,O): _
```

If the boot switches are set for a device boot, one of the following messages will appear: "Booting from Floppy" or, if MACSbug ROMs are installed, "Booting from MACSbug."

If booting is successful, the operating system will be loaded along with full drivers for the I/O devices, a character set for the display, and a full keyboard map.

5.1.4 Self Test Error Codes

In the case of a system test failure, performing the checks in this section may isolate the problem. The test number and their associated system test failures are as follows:

- Test 1—UART Failure
- Test 2—PROM Checksum Failure
- Test 3—Static RAM Test Failure
- Test 4—Dynamic RAM Test Failure
- Test 5—Dynamic RAM Test Failure
- Test 6—Slot Device not Ready Failure
- Test 7—OMNINET Host Number Duplicated

If system errors 1 through 5 are indicated, power off the Concept and remove the drawer from the base unit. Reseat all socketed chips and reassemble the base unit. Power the Concept on again and check for system errors. If problems persist, substitute suspect components with known good components (UARTs, PROMs, static RAMs). A more detailed description of the Self Tests are described below.

NOTE:

There will be some instances where a failure may inhibit these tests. In cases such as these a MACSbug kit, available from Corvus, is recommended. This kit consists of a pair of programmed EPROMs and a user's guide. MACSbug may be used as a 68000 monitor program. It allows a user to set and display the contents of memory, set and display address and data registers, and allows the user to program with the 68000 instruction set by entering the hexidecimal equivalents.

Test 1

Test 1 failure indicates that either a data communication or the keyboard UART failed to respond in the desired way. The error message will not specify which UART is bad. Level 2 troubleshooting will be necessary to find the defective UART using a MACSbug routine. (See Level 2 Troubleshooting in Section 5.2).

If you do not have Level 2 capabilities, replace the Processor Board from your spares kit. Refer to Section 3.5 of this manual for Disassembly and Assembly instructions.

2. Test 2 failure indicates that an invalid code was detected in the boot PROMs. If this error is indicated remove the tray from the base and inspect for unseated PROMs or bent pins. If no visible damage is evident, replace ROM0-U and ROM0-L one at a time.

3. Test 3

   Test 3 failure indicates that the static RAM is defective. The test involves two parts, a walking bit test and a marching bit test. There is only one static RAM installed in the Concept. If after replacing the RAM the test still fails, Level 2 troubleshooting will be necessary requiring MACSbug routines to diagnose the failure.

   If you do not have Level 2 capabilities, replace the Processor Board. Refer to Section 3.5 of this manual for Disassembly and Assembly instructions.

4. Test 4

   Test 4 is used to test the dynamic RAM. Like the static RAM test, it has two parts. The first part exercises RAM by walking a bit throughout memory. The second part of the test is a marching bit test. If Test 4 fails there will be no indication of where or how the test failed. Level 2 troubleshooting will be necessary. MACSbug routines enable a technician to read and write various patterns to all locations of RAM.

   If you do not have Level 2 capabilities, replace the Memory Board. Refer to Section 3.5 of this manual for Disassembly and Assembly instructions.

5. Test 5
   Test 5 is used to test dynamic RAM differently than in Test 4. In this test an incrementing pattern is written to all locations of memory. Again, this test will only indicate that an error exists. To troubleshoot further, Level 2 troubleshooting is required.

   If you do not have Level 2 capabilities, replace the Memory Board. Refer to Section 3.5 of this manual for Disassembly and Assembly instructions.

6. Test 6
   Test 6 is used to examine the 50-pin I/O slots for known devices. The test queries slot #1 for the interface's PROM code. The test then proceeds to compare that code with the known code for a local disk or a Corvus Floppy Disk Drive, in that order. If the comparison fails to match the test then it proceeds to check the next slot's device. Once the test finds a code that it can identify it jumps to a subroutine. This subroutine is used to sync with the device. If the subroutine fails to sync with the device, the message "SYSTEM TEST ERROR 6" is returned. In this case, power the system down and back up, paying special attention to the devices coming ready. If all peripherals are ready, the Concept may not be communicating with them. Check for correct slot insertion. Replace the interface board and cable with known good ones. If System Test 6 still fails, replace peripherals one at a time with known good replacements. If these procedures do not remedy the problem, Level 2 troubleshooting will be required.

   If you do not have Level 2 capabilities, replace the Processor Board. Refer to Section 3.5 of this manual for Disassembly and Assembly instructions.

7. Test 7
   Test 7 will verify that the OMNINET host number is unique. This routine will store the host number into data register DO. A WHO command is then sent across the network, checking the active stations on the network. If the host number is duplicated the routine will indicate a System Test failure 7. Consult the Corvus OMNINET Disk Installation Guide for instructions for setting network device addresses.

   If the problem is still not found, replace the Processor Board. Refer to Section 3.5 of this manual for Disassembly and Assembly instructions.

5.1.5 Boot Problems

There are four boot options available to the user:

- Debug (D)—MACSbug Debugger
- Floppy (F)—Floppy Drive
- Local (L)—Corvus Hard Disk Drive
- OMNINET (O)—Corvus Systems OMNINET local network

If a boot error is encountered, perform the following checks to verify the correct set-up procedures:

1. Boot Switches
   Verify that the boot switches are set properly for the boot device. (See Figures 17 and 18). For example switches 1 and 2 should be off to boot from OMNINET. Switch 1 should be on and switch 2 off for a flat cable boot. If the switch settings are correct proceed to the next step.

   The layout of the Processor Board for Revision 03 of the Corvus Concept is different than those of later Revisions (04, etc.). The boot microswitches have been relocated. The new location should be noted.

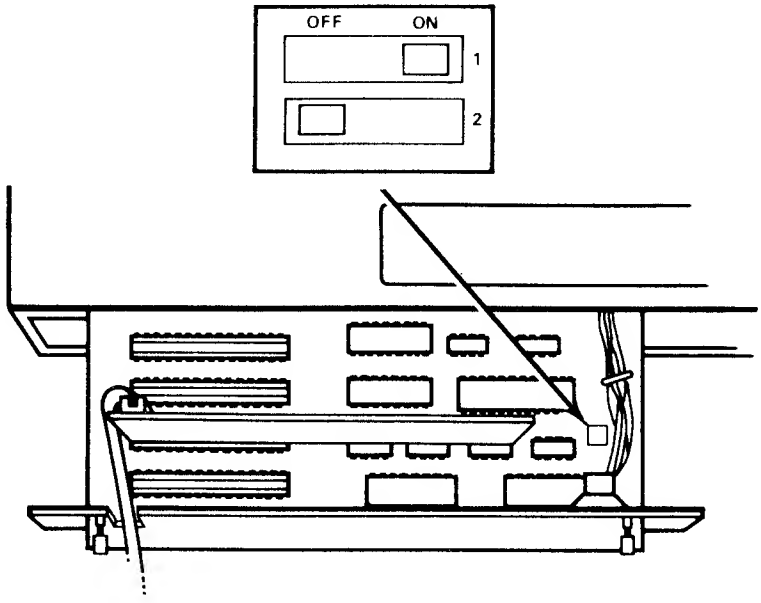


Figure 17. Rev 03 Boot Switch Settings

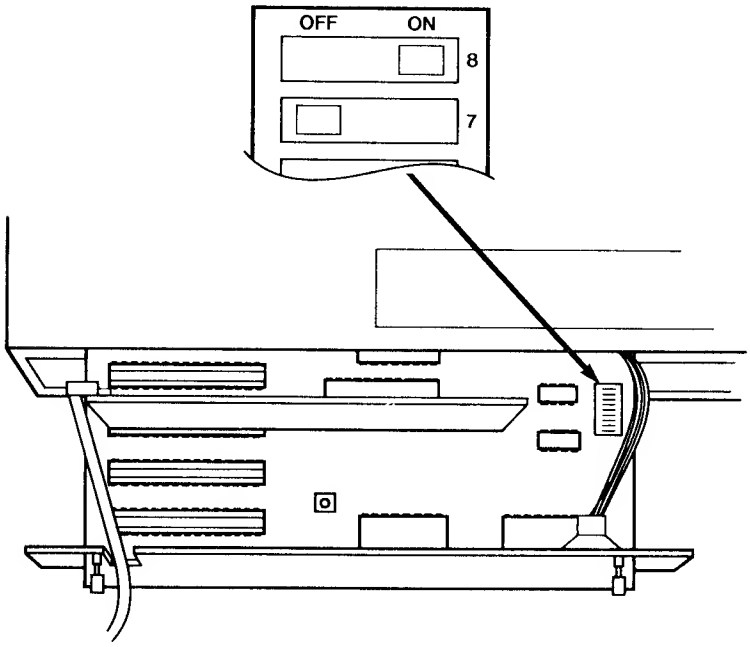


Figure 18. Rev 04 Boot Switch Settings

If the hardware is available, change the switch settings and boot from a different device. If the change results in a successful boot, the previous boot device may be bad or the I/O buffers on the Processor Board related to that device may be defective.

Replace the Processor Board if you do not have Level 2 troubleshooting capabilities. For Disassembly and Assembly instructions, please see Section 3.5 of this manual.

2. Flat Cable Boot
When a flat cable interface will not boot the Corvus disk drive, verify that the interface is correctly installed. Refer to the Corvus Concept Workstation Installation Guide for detailed procedures. A programmed EPROM is required on the interface card in order to be recognized as a valid Corvus disk interface.

3. OMNINET Boot
If the Concept will not boot from OMNINET, ensure that each Concept has a unique host number. The Disk Server should have a host number of zero. Refer to the Corvus OMNINET Installation Guide for hardware set-up instructions.

If the OMNINET boot error persists, Level 2 troubleshooting will be necessary. If you do not have this capability, replace the Processor Board according to the instructions outlined in Section 3.5 of this manual.

4. Floppy Boot
In the event that a Floppy Drive boot error is encountered, refer to the Corvus Concept Floppy Drive Installation Guide to ensure that the proper installation procedures have been followed. After verifying correct installation, try to reboot from the Floppy Disk Drive.

If it stills fails, refer to the Floppy Drive Service Manual for Level 2 floppy drive service procedures.

5.2 Level 2 Troubleshooting

This level of troubleshooting is recommended for in-depth troubleshooting of the Processor Board and Memory Board. It requires a knowledge of digital troubleshooting techniques and an understanding of assembly language.

The Corvus Concept utilizes the Motorola 68000 Microprocessor and its monitor program, MACSbug, for manipulation of the processor during debug. MACSbug may be purchased from Corvus Systems. Sample routines may be found in Appendix E.

In order to facilitate troubleshooting to the component level, we have identified Test Points on the Processor and Memory Boards. A photograph of these Test Point signals and of a logic analyzer showing their relationships appear in Appendix C.

5.2.1 MACSbug Installation Procedures

1. Power-off the Concept base and display.
2. Disconnect the keyboard cable, display monitor cable, and the OMNINET tap cable. Open the drawer of the base unit and remove the power supply cables connected at locations labeled J8 and J1 on the Processor Board and the Memory Board respectively. Remove any tap cables or interface cards which are currently in the drawer.
3. Lift up on the drawer assembly and completely remove it from the base unit.

NOTE:

The layout of the Processor Board for Revisions 03 of the Corvus Concept is different than that of later Revisions (04, etc.). For this installation procedure, the location of the microswitches and the ROM and RAM sockets should be noted. Both Rev 03 and Rev 04 procedures are described.

Revision 03

4. Locate the Boot ROMs on the Processor Board at U706, ROM0U, and U711, ROM0L. Remove the ROMs at these locations if they are not version 0.5 or later. Place a ROM labeled CC 0.5 H or later in location U706 and the ROM labeled CC 0.5 L or later in location U711 on the Processor Board. (See Figure 19.)

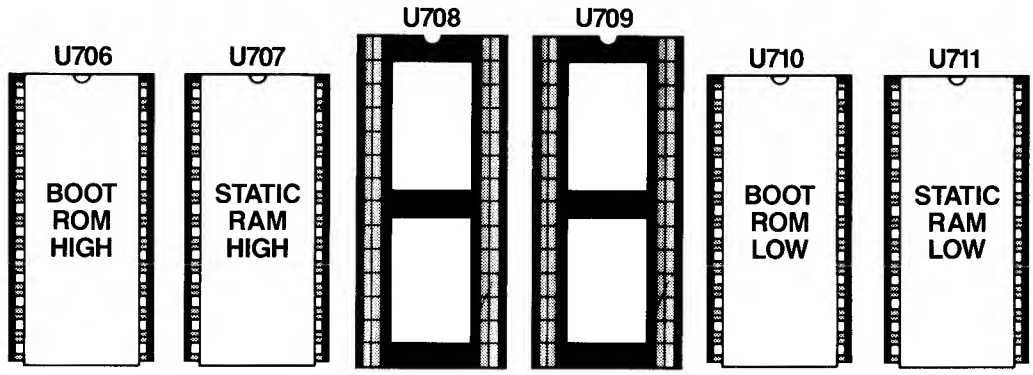


Figure 19. REV 03 ROM and RAM Locations

5. The boot microswitches, located across from the I/O slots on the Processor Board, should be set as indicated in Figure 17.

6. Place the ROM labeled MACSbug 2.0 L in location U709. Place the ROM labeled MACSbug 2.0 H in location U708 of the Processor Board. The MACSbug ROM sockets are 28-pin sockets, and the MACSbug ROMs are 24-pin devices. The sockets should have the top four pin locations unused (i.e. pins 1,2,27 and 28). Figure 19 depicts proper installation.

Revision 04 (and later)

4. Locate the Boot ROMs on the Processor Board at U706, ROM0L, and U710, ROM0U. Remove the ROMs at these locations if they are not version 0.5 or later. Place a ROM labeled CC 0.5 H or later in location U706 and the ROM labeled CC 0.5 L or later in location U706 on the Processor Board. (See Figure 20.)

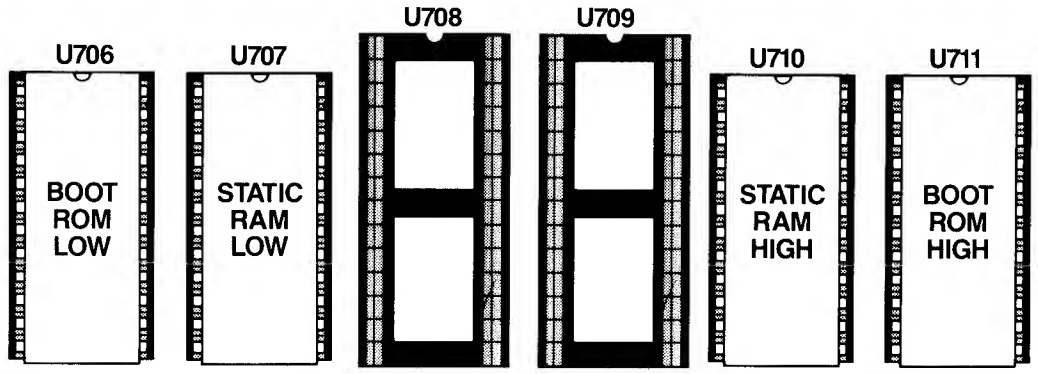


Figure 20. Rev 04 ROM and RAM Locations

5. Set the microswitches, which are located across from the I/O slots on the Processor Board as indicated in Figure 17.
6. Place the ROM labeled MACSbug 2.0 L in location U709. Place the ROM labeled MACSbug 2.0 H in location U708 of the Processor Board. The MACSbug ROMs are 24-pin devices. The sockets should have the top four pin locations unused (i.e. pins 1,2,27 and 28). Figure 20 depicts proper installation.
7. Reconnect the cable from the speaker tray to the connector labeled J7 on the Processor Board, making sure the cable is routed down through the back side of the drawer and inside the standoff supporting the Memory Board.
8. Replace the drawer into the base unit and position the two power supply cables along the speaker tray channel to prevent chaffing of the cables. Reconnect the power supply cables to J8 on the Processor Board and J1 on the Memory Board.
9. Reconnect any tap cables or interface cards originally within the drawer.
10. Power on the display and then the base unit. The Concept will emit a beep, and then request input from the user regarding the boot device as follows:

    Select the device : (D,F,L,O) :

    D—Debug (MACSbug)
    F —Floppy Disk Drive
    L —Local Disk Drive
    O—OMNINET Drive
11. Select your normal disk boot option to run a quick check of the unit. If the unit does not complete the boot, check the ROM locations and verify that all pins of the ROMs are installed correctly. Repeat the procedure until the system boots. If problems persist, contact Corvus Customer Service.

5.2.2 Communicating with MACSbug

Communication with MACSbug is performed through the two serial ports on the back of the Corvus Concept. When used with MACSbug, Port 1 has a default data rate of 9600 baud, parity is disabled and an 8-bit character size is assumed. An ASCII terminal must be attached to Port 1 with a null modem cable. This terminal is the MACSbug console.

MACSbug supports Port 2 as a standard RS-232C data terminal connector with a default data rate of 4800 baud, parity disabled and an 8-bit data character size. Port 2 can be used to communicate with a host computer, a printer or other serial device.

This two port communication arrangement allows the Corvus Concept to be placed in series with an ASCII terminal and a host computer. The transparent mode of MACSbug can be used to bypass the Corvus Concept. A program may be created on the host computer using the ASCII terminal and, when the program code file is generated, downloaded into the Corvus Concept for execution and debugging. This does not require the reconfiguration of the cabling.

5.2.3 Operating Procedures

After the MACSbug ROMs have been installed, MACSbug can be entered before the Corvus Concept operating system is booted as follows:

1. Connect an ASCII terminal to Port 1 of the Corvus Concept.
2. Ensure that the Concept boot switches are both in the ON position.
3. Power on the Corvus Concept.
4. Select option D, for Debugger, when prompted.

MACSbug will initialize and display on the ASCII terminal connected to Port 1 with the following message:

```
MACSbug 2.0
*
```

If these two lines do not print out, perform the following:

1. Check to see that the ASCII terminal is attached to RS-232C Port 1 using a null modem cable.
2. Ensure that the terminal's baud rate is set to 9600, parity is disabled, and an 8-bit character size is selected.

5.2.4 MACSbug Routines

MACSbug routines are useful for writing loop-back tests to diagnose static RAM, and I/O addresses. Some of the most commonly used mnemonics are:

- SM —Set Memory
- DM—Display Memory
- OP —Open address

The recommended memory starting location for static RAM is $700.

MACSbug is a versatile tool for use in troubleshooting. Modifications should be made to the sample routines in Appendix E to fit specific needs. MACSbug routines listed are in assembly code.

5.3 Component Level Troubleshooting

After isolating the failure at the board level, further troubleshooting may be desired. With the aid of troubleshooting guides, timing diagrams, and Test Points a technician may troubleshoot down to a defective component. The Processor Board contains 24 Test Points for various signals. (See Appendix C-1.)

CAUTION:

The Processor Board consists of many layers. Damage will occur to the board if proper soldering procedures are not followed.

5.3.1 Processor Signal Descriptions

A few major signals should be tested before checking the Test Points. The Concept will not operate unless these signals are present.

1. Clock Signals
   If clock signals are incorrect or absent, a bad buffer IC, U109, 74LS04 may be present. If the inputs of this chip are bad a defective cable or Memory Board may be responsible. Proceed to the memory Section 5.3.3.

   With an oscilloscope measure the signals at locations U109 pins 2 (16MHz), 6 (8MHz, Test Point 3), and 8 (1MHz). These clock signals are described in the following Section, 5.3.2, and illustrated in Appendix C-1. Timing relationships of these signals, can be found in Appendix D-1.

2. RESET
   On initial power-up, the hardware generates a momentary reset. This bidirectional signal can be generated internally by the processor, or through external hardware. If this line is stuck low, check the input to the buffer U304 pin 11.

   With an oscilloscope measure the RESET signal at location U402 pin 18. The RESET signal is described in the following Section and a photograph of the signal is included in Appendix C-1.

5.3.2 Processor Test Points

The Processor Board has designated Test Points to facilitate troubleshooting.

Test Point	Signal Name	Apprx. Location
1	DMAGO2	U104-9
2	DMAEN	U104-5
3	8M	U103-6
4	TXENA	U114-4
5	IN/OUT	U110-12
6	NTACK	U411-5
7	TXD	U110-6
8	DTACK	U306-10
9	RAMSEL	U203-8
10	NRAMACK	U205-12
11	NAS	U307-14
12	NOMNI	U109-32
13	NOMINT	U304-8
14	HALT	U405-10
15	NWRITE	U603-11
16	IPL1	U404-7
17	IPL2	U404-6
18	IPL0	U404-9
19	DS	U308-8
20	NDTACK	U510-6
21	NSRO	U705-14
22	NDEVS	U704-4
23	NKBD	U705-15
24	NSR1	U705-13

Table 4. Processor Board Test Points, Rev 04 & 05

The Test Points and their signals are described in the following paragraphs. An "N" prefix on a signal name indicates that it is asserted when the signal goes low. See Appendix D-1 for proper timing relationships. Signal waveforms and Test Points are depicted in Appendix C-1.

1. Test Point 1—DMAGO2
   When asserted, the DMAGO2 signal indicates that OMNINET is in the process of doing a DMA operation. If asserted, OMNINET has total control over the memory address and data bus. If the processor attempts to access memory it will go into a wait state until the DMA operation is complete.

2. Test Point 2—DMAEN
   When the DMAREQ is asserted, it is latched into a JK flip-flop on the next 16M clock pulse. The output of this latch is the signal DMAEN.

3. Test Point 3—8M
   The 8M signal is the system clock. This clock is generated on the Memory Board and supplied to the Processor Board by means of a flat cable. The signal is then inverted and applied to the 68000 microprocessor chip.

4. Test Point 4—TXENA
   The TXENA signal is used by OMNINET. When the Concept requires data to be transmitted across the twisted pair cable of OMNINET, the 6801 asserts this signal. The TXENA enables a transmitter chip, 75174. This allows data to flow from the Advanced Data Link Controller, ADLC, to the RS-422 connector.

5. Test Point 5—IN/OUT
   The IN/OUT signal is used as the R/W line for the ADLC chip in the OMNINET. This signal controls the direction of the data flow on the data bus when enabled by EOUT and NCS.

6. Test Point 6—NTACK
The memory generates a data acknowledge, NTACK when RAMSEL is negated or when NRAMACK is asserted.

7. Test Point 7—TXD
TXD is the serially transmitted data from the OMNINET ADLC chip. After the signal TXENA is asserted, the data is transmitted across the twisted pair cable.

8. Test Point 8—DTACK
With an oscilloscope measure the signal at location U605 pin 5, Test Point 20. If the MC68000 does not receive a low signal on this line, it will go into a wait state. Check the input signals on U605.

9. Test Point 9—RAMSEL
The Memory Board requires RAMSEL before an access can start. RAMSEL must then be negated before a new access can start. RAMSEL is derived from either the 68KRAMSEL signal or the DMAGO2 signal depending on which device has control over the memory bus.

10. Test Point 10—NRAMACK
The memory data acknowledge signal, RAMACK, is asserted when the signal NCAS (see memory section) goes high. Once initiated, memory cycles occurs until NRAMACK is asserted. NRAMACK signals that the data in an access has been latched by the 68000.

11. Test Point 11—NAS
This signal, when asserted, signifies a valid address is on the address bus.

12. Test Point 12—NOMNI
In order for the processor to give OMNINET commands, the processor places a byte of data on the data bus and then strobes NOMNI. When this has occurred for three strobes, OMNINET uses the three bytes of data as an address.

13. Test Point 13—NOMINT
The Concept processor recognizes seven levels of interrupts. OMNINET utilizes a level three interrupt. The OMNINET 6801 will generate an interrupt to the 68000 when a transaction is complete or when an error is encountered.

14. Test Point 14—HALT
HALT is a bidirectional signal that can be asserted either by the processor or by external software. When this signal is asserted low, all control signals are inactive and the data and address buses are put in a high impedance state.

15. Test Point 15—NWRITE
This signal identifies the data bus transfer as a read or write operation. When the signal goes low, a write is signified.

16. Test Points 16, 17 and 18—IPL0, IPL1, IPL2
These three input pins indicate the encoded priority level of the device requesting an interrupt. Level zero indicates no devices interrupt. A level of seven, not used in the Concept at this time, is reserved for Non-Maskable Interrupts. The least significant bit is contained in IPL0 and the most significant bit contained in IPL2. See Table 4 for a list of devices and interrupt levels.

17. Test Point 19—DS
This signal is the result of a logical NAND operation between the upper data strobe (NUDS) and lower data strobe (NLDS). The DTACK delay is cleared when the data strobe, DS, is negated.

18. Test Point 20—NDTACK
NDTACK indicates the completion of a data transfer. When the processor recognizes NDTACK on a read cycle, data is latched and the bus cycle is terminated. When NDTACK is recognized on a write cycle, the bus cycle is terminated. Memories and I/Os of different speeds are accommodated by delaying DTACK until the access is complete.

19. Test Points 21 and 24—NSR0, NSR1
NSR0 and NSR1 are the chip selects for two Synertek SY6551 UARTs. The UARTs control data communications for the RS-232C Port 0 and Port 1. (See Appendix H-2.)

20. Test Point 22—NDEVS
NDEVS is used as an enable for the addressable I/O slot. The range of addresses is from 30021 to 3009F or 30121 to 3019F HEX. Either set of addresses access the same memory locations. All addresses in this range must be odd.

21. Test Point 23—NKBD
NKBD is used as a chip select on the SY6551 UART. This particular UART is used for keyboard communications. The signal is addressable within the range of 30F01 to 30F07 HEX. See the Memory Map chart in Appendix F.

5.3.3 Memory and Video Controller Test Points

The memory and video controller contains the necessary circuitry for system timing and clock generation as well as memory addressing and data control. This board supplies the necessary signals to the video monitor such as video data, sync pulses, and horizontal and vertical blanking pulses. Some key signals are described in the following paragraphs. See Table 5 for actual signal locations and Appendix C-2 for Test Point locations.

Signal Name	Board Location
16M	U101-1
HSYNC	U105-4
VSYNC	U105-2
ENVID	U301-15
LOADVID	U504-2
NVIDTIME	U401-7
MUX	U405-14
NRASTIME	U405-15
NCASTIME	U405-13
68K	U305-3
NWL, NWU	U305-3,11

Table 5. Memory and Timing Signal Locations

1. 16M
This 16MHz signal is the basis of all timing within the Concept. This clock signal is generated by an oscillator at a frequency of 16.364 MHz. Counters divide this signal to frequencies of 8 MHz, 1 MHz and 35 KHz.

2. HSYNC
The HSYNC is generated on the Memory Board by a horizontal counter, HCTR, Revision 7. This signal is a 3 μs pulse which is used to hold the video screen in place horizontally.

3. VSYNC
VSYNC similar to the HSYNC, is generated on the Memory Board by an 82S153. It locks the video screen in place vertically. The frequency of this signal will differ between the 50 Hz and 60 Hz monitors. Jumper TF determines the vertical frequency. VCTR, the vertical counter, and HCTR can be reprogrammed. They are not EPROMS but have sufficient spare states to be reprogrammed.

4. ENVID
   This signal blanks the video screen when negated. The blanking is accomplished by clearing the video data shift registers. The signal is output from the HCTR and VCTR.

5. LOADVID
   LOADVID loads data from the RAM into the video shift registers. This pulse occurs close to the end of NVIDTIME. See Appendix D for the proper timing relationships.

6. NVIDTIME
   When the video requires a data input or refreshing, the signal NVIDTIME is asserted. NVIDTIME is 1.02275 MHz, asserted and negated for a total of 488.87 ns. Video access and processor access of memory cannot occur at the same time. The processor may or may not require the memory base, but video time must be consistent and accurate.

7. NMUX
   During NVIDTIME, the video address counter is selected to address the memory. The signal NMUX determines whether the upper or lower part of the address goes to the memory to be stored by RAS and CAS.

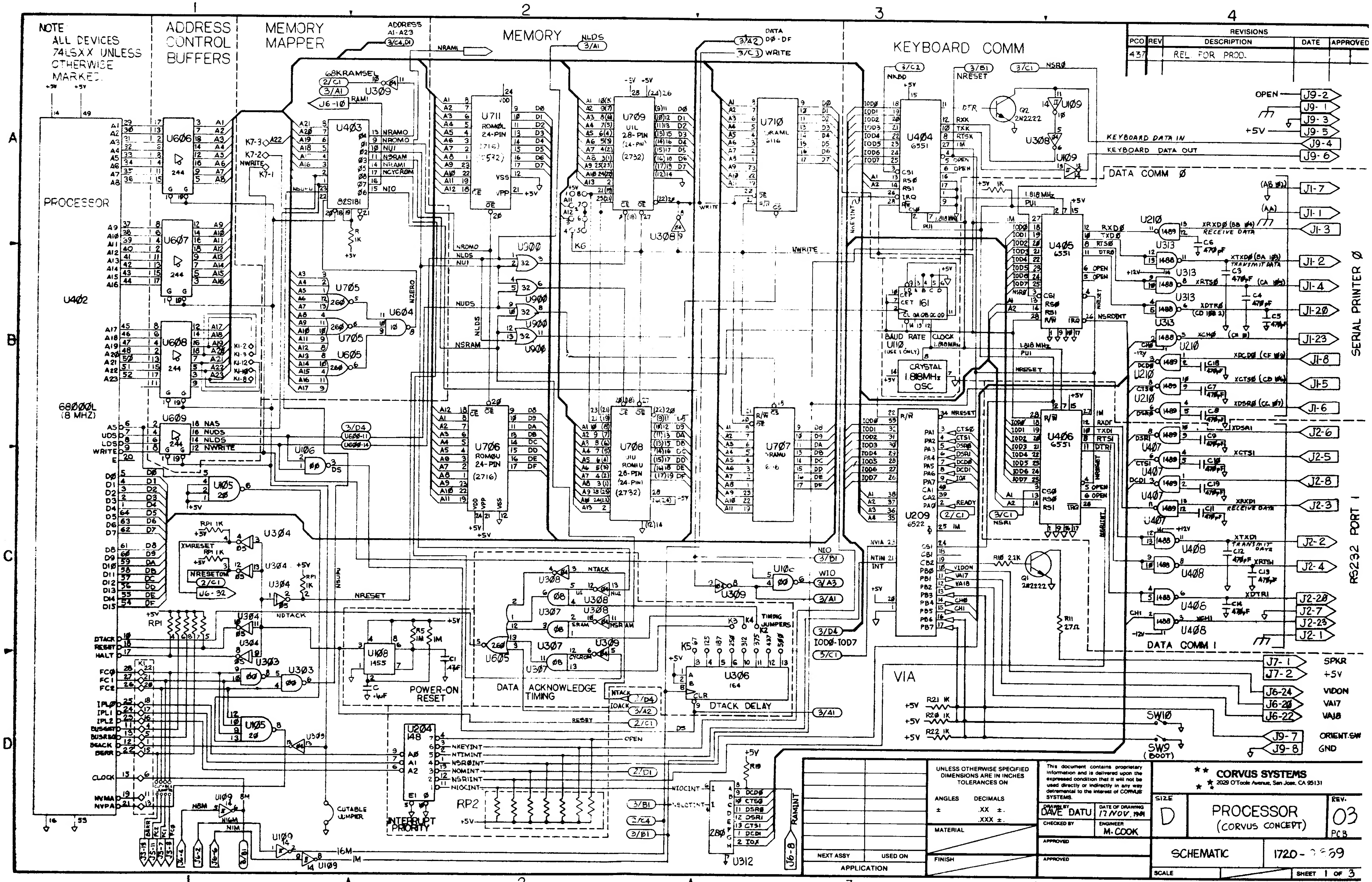
   The signal NRASTIME is derived from the horizontal counter. It is used in conjunction with the Bank Select to create the Row Address Select, RAS, for the various banks of memory.

9. NCASTIME
   NCASTIME is derived from the vertical counter. It is used with the Bank Select to create the Column Address Select, CAS, for the various banks of memory.

10. 68K
    The 68K signal allows the memory to do a read or write cycle for the processor. The processor cannot access at this time. NVIDTIME and 68K cannot occur simultaneously.

11. NWL, NWU
    These signals are used as the R/W lines for the upper and lower RAM banks and are active low signals.

APPENDIX A
SCHEMATICS AND ASSEMBLY DRAWINGS


NOTE
ALL DEVICES 74LSXX UNLESS OTHERWISE MARKED
ADDRESS CONTROL BUFFERS
MEMORY MAPPER
MEMORY
KEYBOARD COMM
PROCESSOR
U402
68000L (8 MHZ)
POWER-ON RESET
DATA ACKNOWLEDGE TIMING
DTACK DELAY
INTERRUPT PRIORITY
VIA
DATA COMM 0
DATA COMM 1
SERIAL PRINTER 0
RS232 PORT 1
KEYBOARD DATA IN
KEYBOARD DATA OUT
BAUD RATE CLOCK
CRYSTAL 1.8MHz OSC
TIMING JUMPERS
CUTABLE JUMPER
SPKR
+5V
VIDON
VAI7
VAI8
ORIENT.SW
GND
REVISIONS
PCO | REV | DESCRIPTION | DATE | APPROVED
437 | | REL FOR PROD.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON
ANGLES ±
DECIMALS .XX ± .XXX ±
MATERIAL
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NEXT ASSY
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DATE OF DRAWING 17 NOV. 1981
CHECKED BY
ENGINEER M. COOK
APPROVED
CORVUS SYSTEMS
2029 O'Toole Avenue, San Jose, CA 95131
SIZE D
PROCESSOR (CORVUS CONCEPT)
REV. 03 PCB
SCHEMATIC
SCALE
SHEET 1 OF 3

REVISIONS				
PCO	REV	DESCRIPTION	DATE	APPROVED
437		see page 1 of 3		

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FINISH	CHECKED BY	ENGINEER M. COOK		
NEXT ASSY USED ON APPLICATION	APPROVED		SCHEMATIC	1720-01869
	APPROVED		SCALE	SHEET 3 OF 3

REVISIONS				
PCO	REV	DESCRIPTION	DATE	APPROVED
437	A	PEL FOR PRINT	7-7-82	

POWER SUPPLY DECOUPLING:
Ø.1µF PER 5 LS DEVICES
Ø.1µF FOR EVERY DEVICE GREATER OR EQUAL TO 20 PINS

NOTE: ALL TTL DEVICES ARE 74LSXXX UNLESS OTHERWISE NOTED.

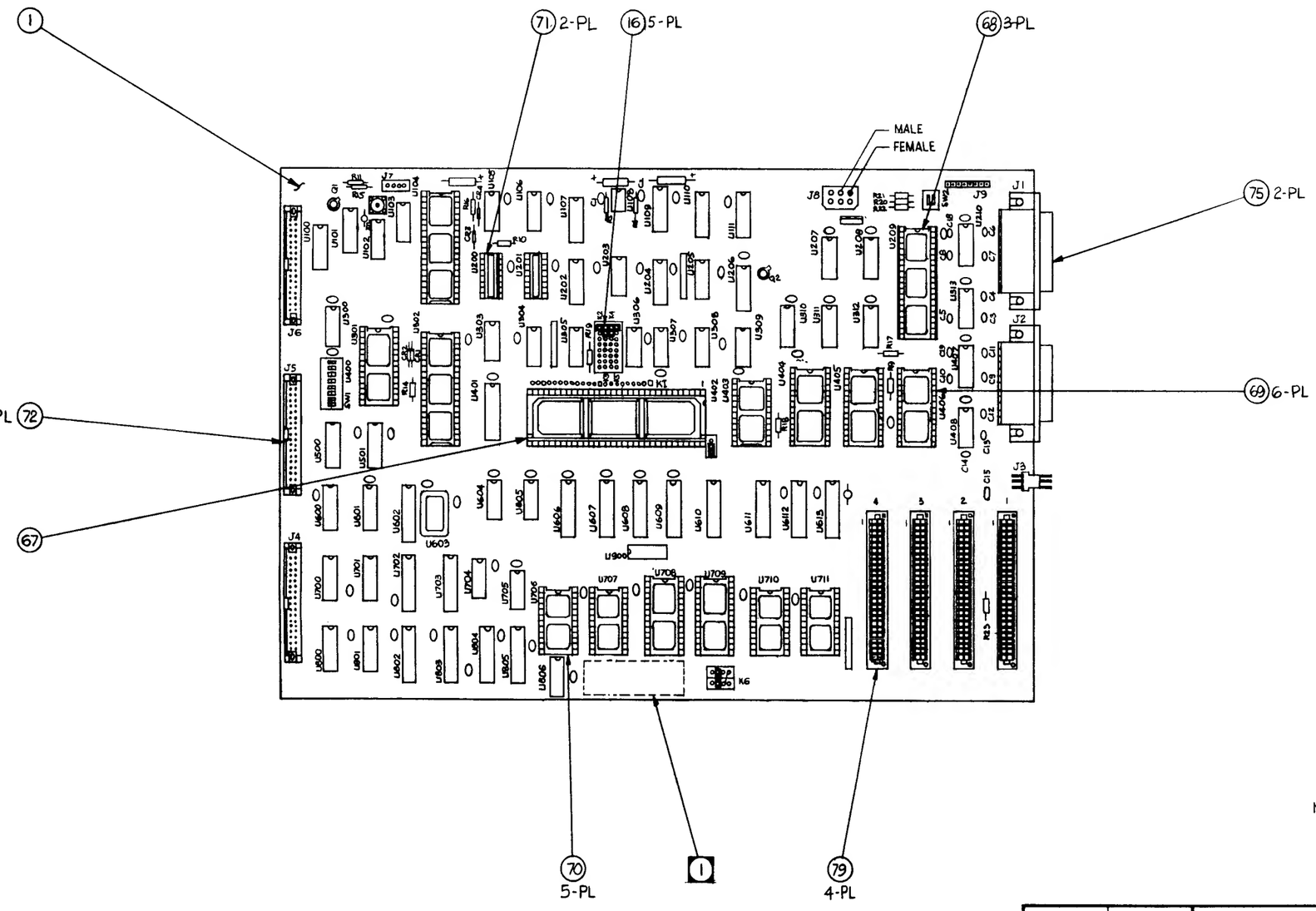
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON
ANGLES ± N/A DECIMALS .XX ± N/A .XXX ±
MATERIAL N/A
FINISH N/A
NEXT ASSY | USED ON
APPLICATION

DRAWN BY DAVE DATU | DATE OF DRAWING 06-25-82
CHECKED BY | ENGINEER MIKE COOK
APPROVED
APPROVED

CORVUS SYSTEMS
2029 O'Toole Avenue, San Jose, CA 95131

SIZE D | CORVUS CONCEPT PROCESSOR | REV. 03 PCB
SCHEMATIC | 1720-01869
SCALE NTS | SHEET 2 OF 3

REVISIONS				
PCO	REV	DESCRIPTION	DATE	APPROVED
437	A	REL FOR PROD	7-7-82	
472	B	REL NEW ROOT PROMS	7-14-82	



2 - SQUARE PADS INDICATES PIN 1 OF IC, POSITIVE END OF CAP., EMITTER. OF TRANSISTOR.

(1) PERMANENTLY MARK OR IDENTIFY REV. LEVEL APPROX. WHERE SHOWN.

NOTES: UNLESS OTHERWISE SPECIFIED.

REV 03 PCB

8010-08080	ELECT. DRWR.
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON
ANGLES ± DECIMALS .XX ±. .XXX ±.
MATERIAL
FINISH

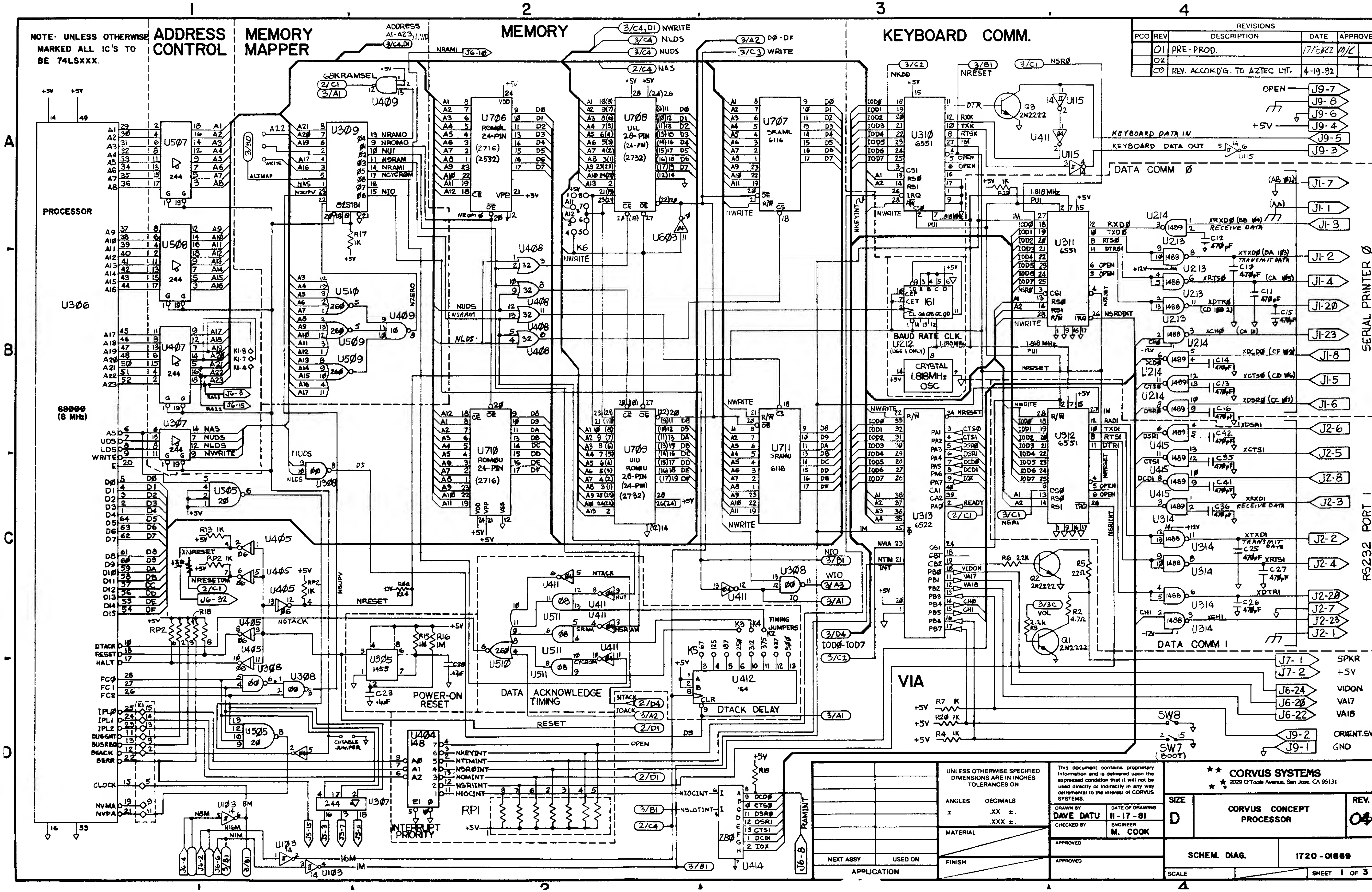
DRAWN BY D. DATU | DATE OF DRAWING 02-03-82
CHECKED BY | ENGINEER L. FROHMAN
APPROVED
APPROVED

CORVUS SYSTEMS
2029 O'Toole Avenue, San Jose, CA 95131

CORVUS CONCEPT PROCESSOR BOARD | REV. B

ASSEMBLY DWG 8010-08024

SCALE FULL | SHEET | OF |


NOTE: UNLESS OTHERWISE MARKED ALL IC'S TO BE 74LSXXX.
ADDRESS CONTROL
MEMORY MAPPER
MEMORY
KEYBOARD COMM.
REVISIONS
PCO REV DESCRIPTION DATE APPROVED
01 PRE-PROD.
02
03 REV. ACCORD'G. TO AZTEC LTT. 4-19-82
PROCESSOR
U306
68000 (8 MHz)
DATA COMM 0
SERIAL PRINTER 0
DATA COMM 1
RS232 PORT 1
KEYBOARD DATA IN
KEYBOARD DATA OUT
BAUD RATE CLK.
CRYSTAL 1.818MHz OSC
POWER-ON RESET
DATA ACKNOWLEDGE TIMING
DTACK DELAY
TIMING JUMPERS
INTERRUPT PRIORITY
VIA
SPKR
VIDON
VA17
VA18
ORIENT. SW.
GND
CORVUS SYSTEMS
2029 O'Toole Avenue, San Jose, CA 95131
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON
ANGLES DECIMALS
This document contains proprietary information and is delivered upon the expressed condition that it will not be used directly or indirectly in any way detrimental to the interest of CORVUS SYSTEMS.
DRAWN BY DAVE DATU
DATE OF DRAWING 11-17-81
CHECKED BY
ENGINEER M. COOK
APPROVED
MATERIAL
FINISH
NEXT ASSY
USED ON
APPLICATION
SIZE D
CORVUS CONCEPT PROCESSOR
REV. 04
SCHEM. DIAG.
1720-01869
SCALE
SHEET 1 OF 3

REVISIONS			
PCO REV	DESCRIPTION	DATE	APPROVED
	01	7 FEB 84	MK
	02		
	03 SEE SHT 2 OF 3		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON	This document contains proprietary information and is delivered upon the expressed condition that it will not be used directly or indirectly in any way detrimental to the interest of CORVUS SYSTEMS.	★★ CORVUS SYSTEMS ★★ 2029 O'Toole Avenue, San Jose, CA 95131	
ANGLES ± DECIMALS .XX ±. .XXX ±.	DRAWN BY DAVE DATU — DATE OF DRAWING NOV. 30/84	CORVUS CONCEPT PROCESSOR	REV 04
MATERIAL	CHECKED BY — ENGINEER M. COOK	SCHEMATIC	1720-01869
FINISH	APPROVED	SCALE NONE	SHEET 3 OF 3
NEXT ASSY — USED ON APPLICATION	APPROVED		

REVISIONS				
PCO	REV	DESCRIPTION	DATE	APPROVED
	01	REPLACED SDS on U511	17 FEB 82	MK
	02	ADDED LED TO U302-11 ADDED UG05 TO DMAGO (J5-19)		
	03	CORRECTED BUS LINES BET. U802, U602 & U302.	4-19-82	
	04	①ADDRESS BUS ON 3/D1 CONN. TO ADD. BUS ON 3/C4. ②NLDS & NWRITE CONN. TO ADDRESS BUS ON 3/C3 & 3/C2. ③N1M CHGD. TO 1M ④N1MN CHGD. 1MN ⑤U303 PINS 11,12 & 13 DELETED ⑥NCALM MOVE TO U705 PIN 11 ⑦U705 PIN 7 CONN. TO I/O SLOTS PIN 20.	5-27-82	

U111 (6801-1)

U2Ø8 273 — U2Ø7 273 — U1Ø5 283 — U1Ø6 175 — U1Ø8 374 — U1Ø7 374 — U3Ø4 — U112 — SW1 — DS1 — R1 47ØΩ — R14 10k — U11Ø ADLC — U114 75174 — U113 75175 — U2Ø6 10 MHz — U4Ø3 — U3Ø4 — U2Ø3 — U2Ø5 — U3Ø7 — U1Ø9 MONOCHIP

NOTE: ALL TTL DEVICES ARE 74LSXX UNLESS OTHERWISE NOTED.

POWER SUPPLY DECOUPLING:
Ø.1μF PER 5 LS DEVICES
Ø.1μF FOR EVERY DEVICE GREATER THAN OR EQUAL TO 2Ø PINS.

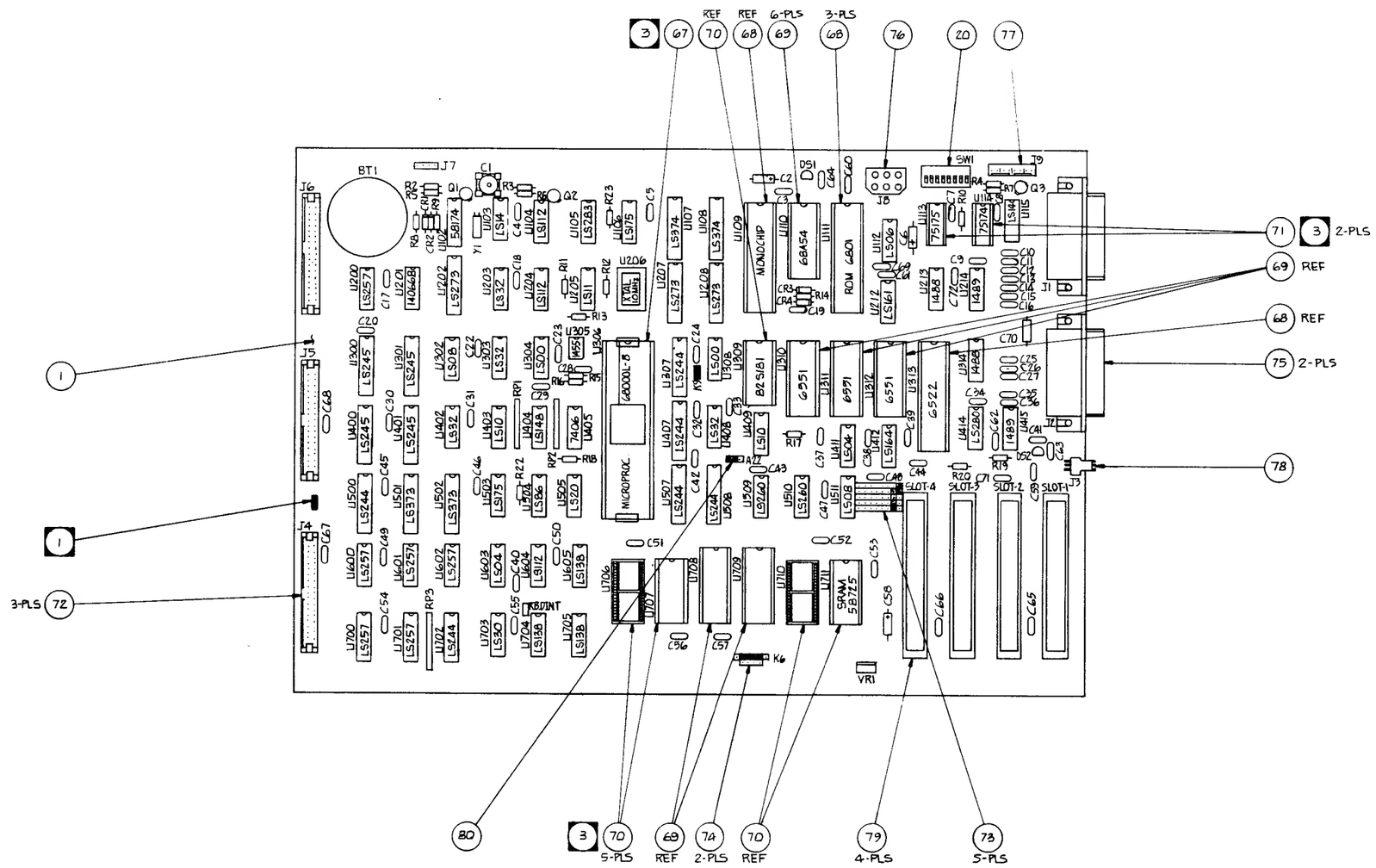
NEXT ASSY	USED ON	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON ANGLES ± DECIMALS .XX ± .XXX ±	This document contains proprietary information and is delivered upon the expressed condition that it will not be used directly or indirectly in any way detrimental to the interest of CORVUS SYSTEMS.
APPLICATION		MATERIAL / FINISH	DRAWN BY DAVE DATU — DATE OF DRAWING NOV. 19, 1981 — CHECKED BY — ENGINEER M. COOK — APPROVED — APPROVED

★★ CORVUS SYSTEMS ★★ 2029 O'Toole Avenue, San Jose, CA 95131

CORVUS CONCEPT PROCESSOR — REV 04

SCHEMATIC — 1720-01869

SCALE NONE — SHEET 2 OF 3



REVISIONS				
PCO	REV	DESCRIPTION	DATE	APPROVED
578	C	ADD. REF. DES.	8-9-82	
579	D	UPDATE (ENG'G)	8-19-82	
669	E	CAP CHNGD - ITEM 7	9-9-82	
678	F	CHNGD ITEMS 84 & 85	10-6-82	
713	G	ADD ITEMS TO LM	10-12-82	
708	H	LM CHNGD ONLY	10-14-82	
710	J	LM CHNGD ONLY	10-14-82	
748	K	CHNGD ITEM 55 (LM)	10-25-82	
773	L	LM / ENG'G CHNGD	11-12-82	
776	M	BOOT PROM CHNGD (LM)	11-12-82	
799	N	ADD ITEM 18 (RN3)	11-19-82	
860	–	RWK INSTR CHNGD ONLY	1-14-83	
/	/	CHNGS - SEE PCO # 860 CHNGD C70 TO 47uF, CHNGD RN3 TO RP3	2-9-83	
/	/	UPDATE (SEE ECO # 860)	2-18-83	
/	/	K6, K9, & A22 REV. -ECO#860	2-23-83	
916	Q	ADD ITEM 96 (LM)	2-18-83	
987	R	REL. OF REV. B PCB	3-11-83	

3 SOCKETS TO BE INSTALLED DURING ASSY. - DEVICES TO BE INSTALLED AFTER PROGRAMMING OR DURING TEST

2 SQUARE PADS INDICATES PIN #1 OF I.C., POSITIVE END CAP

1 PERMANENTLY MARK OR IDENTIFY REV. LEVEL TO BE LOCATED WHERE APPROX. SHOWN

NOTES: UNLESS OTHERWISE SPECIFIED:

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON

ANGLES ± DECIMALS .XX ±. .XXX ±.

MATERIAL

FINISH

DRAWN BY D.D.	DATE OF DRAWING 2-9-83
CHECKED BY	ENGINEER L.FROHNAN
APPROVED	
APPROVED	

CORVUS SYSTEMS
2029 O'Toole Avenue, San Jose, CA 95131

CORVUS CONCEPT PROCESSOR BOARD

REV. R

SIZE D | ASSY. DWG. | P/N 8010-08024

SCALE 1X | SHEET 1 OF 1

HORIZONTAL TIMING

VERTICAL TIMING

RAM TIMING

REVISIONS				
PCO	REV	DESCRIPTION	DATE	APPROVED
418	A	REL FOR PROD.	7-7-82	

VIDEO ADDRESS COUNTER

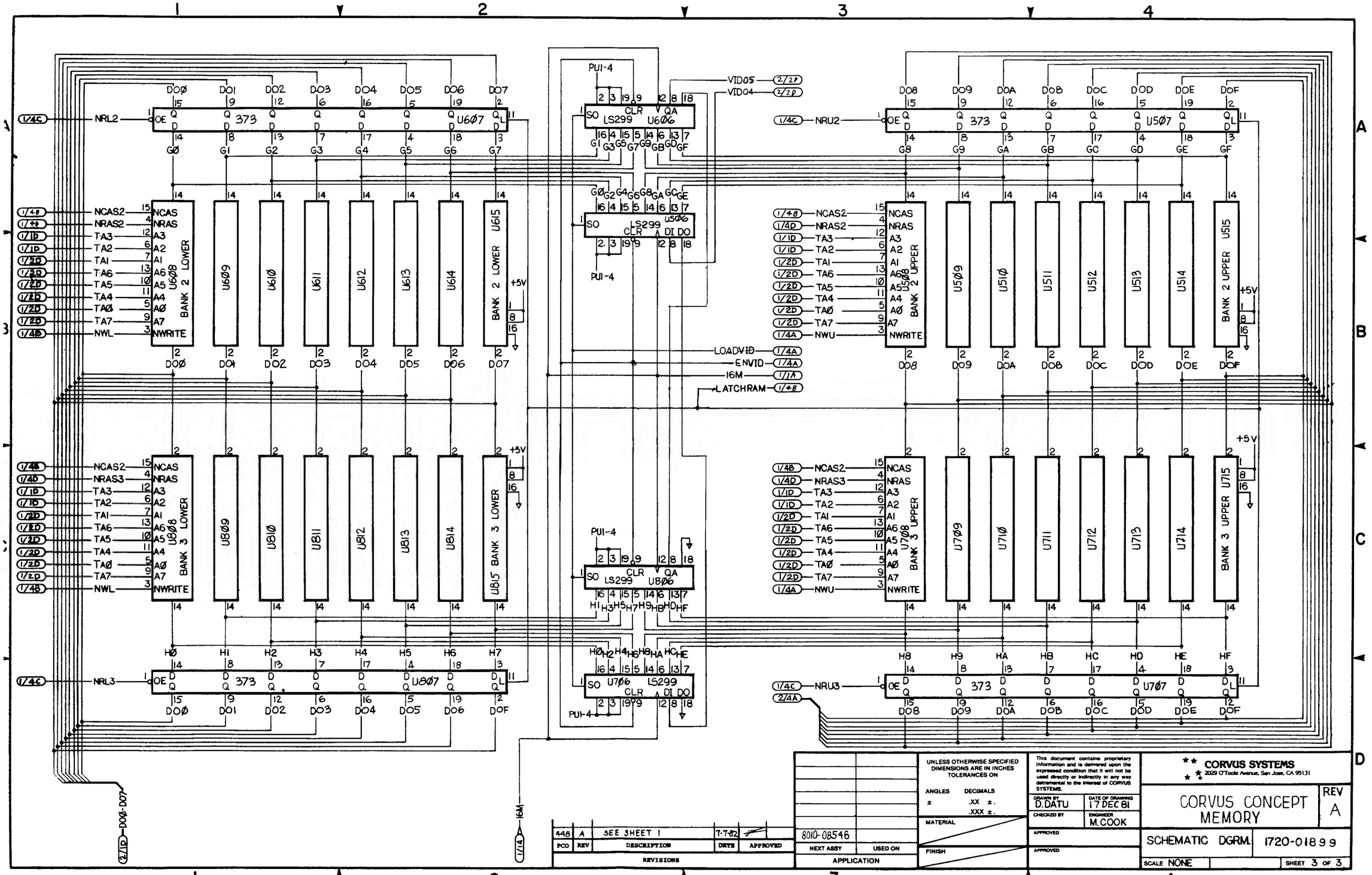
ADDRESS MULTIPLEXING

BANK SELECTION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON ANGLES ± DECIMALS .XX ± .XXX ±	This document contains proprietary information and is delivered upon the expressed condition that it will not be used directly or indirectly in any way detrimental to the interest of CORVUS SYSTEMS.	CORVUS SYSTEMS 2029 O'Toole Avenue, San Jose, CA 95131
MATERIAL	DRAWN BY DAVE DATU	DATE OF DRAWING 01-30-82
FINISH	CHECKED BY	ENGINEER M. COOK
8010-08546 NEXT ASSY / USED ON APPLICATION	APPROVED	APPROVED
	SIZE D	CORVUS CONCEPT MEMORY — REV. A
	SCHEM. DIAG.	1720-01899
	SCALE	SHEET 1 OF 3

REVISIONS				
PCO	REV	DESCRIPTION	DATE	APPROVED
448	A	SEE SHEET 1	7-7-82	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON		This document contains proprietary information and is delivered upon the expressed condition that it will not be used directly or indirectly in any way detrimental to the interest of CORVUS SYSTEMS.	CORVUS SYSTEMS, 2029 O'Toole Avenue, San Jose, CA 95131
ANGLES ± DECIMALS .XX ±. .XXX ±.		DRAWN BY: DAVE DATU; DATE OF DRAWING: 01-30-82; CHECKED BY: ; ENGINEER: M. COOK	SIZE: D; CORVUS CONCEPT MEMORY; REV: A
MATERIAL		APPROVED	SCHEM. DIAG. 1720-01899
FINISH		APPROVED	SCALE: ; SHEET 2 OF 3
8010-08546 NEXT ASSY	USED ON		
APPLICATION			



PCO	REV	DESCRIPTION	DATE	APPROVED
448	A	SEE SHEET 1	7-7-82	

REVISIONS

8010-08546
NEXT ASSY | USED ON
APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON
ANGLES ±
DECIMALS .XX ±. .XXX ±.
MATERIAL
FINISH

DRAWN BY D.DATU | DATE OF DRAWING 17 DEC 81
CHECKED BY | ENGINEER M.COOK
APPROVED
APPROVED

CORVUS SYSTEMS
2029 O'Toole Avenue, San Jose, CA 95131

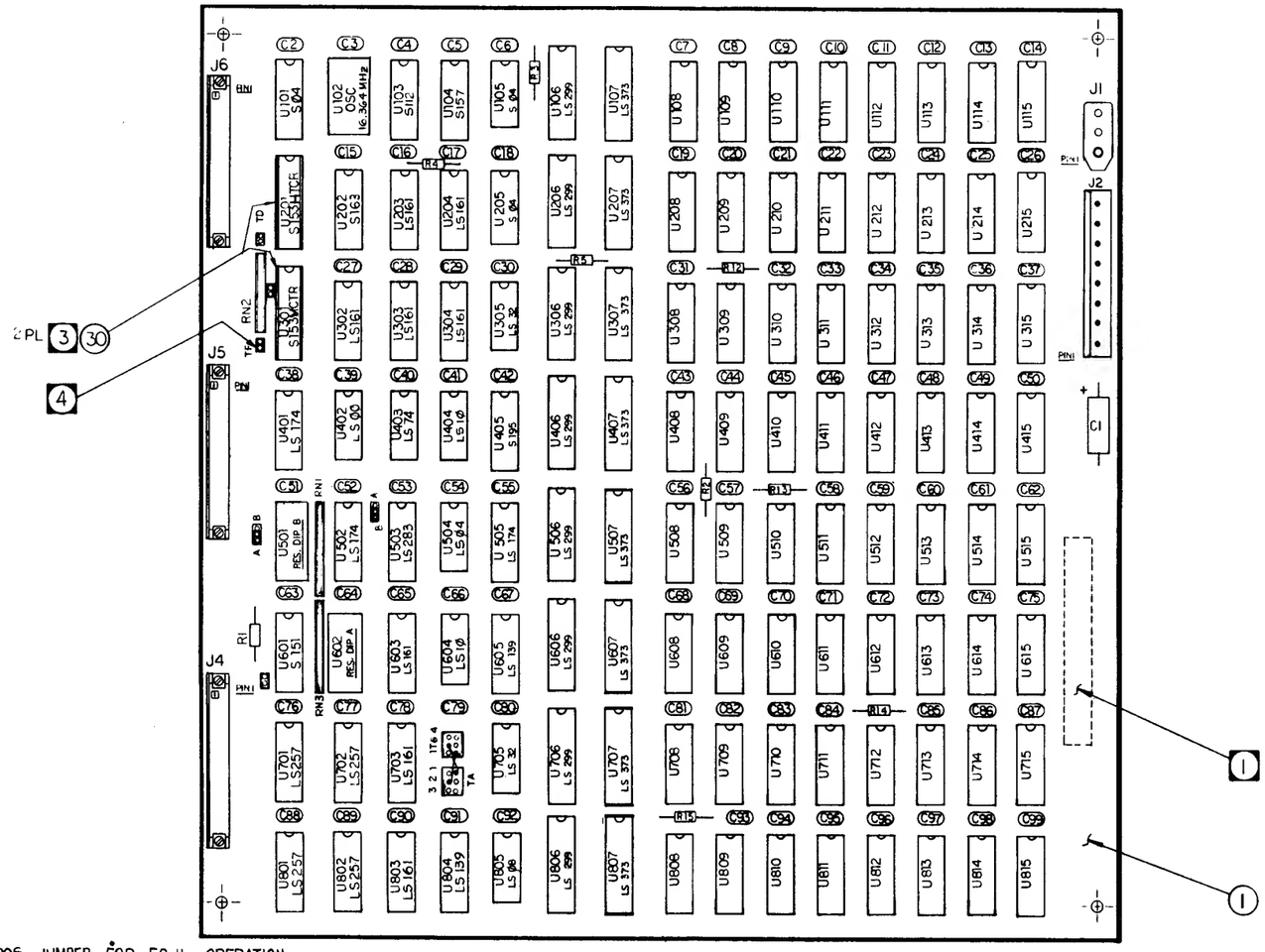
CORVUS CONCEPT MEMORY

REV A

SCHEMATIC DGRM. 1720-01899

SCALE NONE | SHEET 3 OF 3

REVISIONS				
PCO	REV	DESCRIPTION	DATE	APPROVED
498	A	REL FOR PROD	7-8-82	
535	B	ADD REWORK INST	8-6-82	
637	C	CHG ITEM #26	8-26-82	
713	D	ADD ITEMS TO L/M	10-12-82	
771	E	CHG TOLERANCE ON XLTO (LM)	11-12-82	
916	F	ADD ITEM 44 (LM)	2-18-83	



4 INSTALL 2-POS. JUMPER FOR 50 Hz OPERATION.

3 INSTALL SOCKETS DURING ASSY-DEVICES WILL BE INSTALLED AFTER PROGRAMMING OR DURING TEST.

2 SQUARE PAD INDICATE PIN 1 OF IC, POSITIVE END OF CAPACITOR.

1 PERMANENTLY MARK OR IDENTIFY REV. LEVEL APPROX WHERE SHOWN.

NOTES: UNLESS OTHERWISE SPECIFIED.

8010-08670	512K MISC. DRAWER ASSY.
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON

ANGLES ± DECIMALS .XX ±. .XXX ±.

MATERIAL

FINISH

DRAWN BY H. BUI — DATE OF DRAWING 4/20/82

CHECKED BY — ENGINEER L. FRANHAN

APPROVED E. Kent

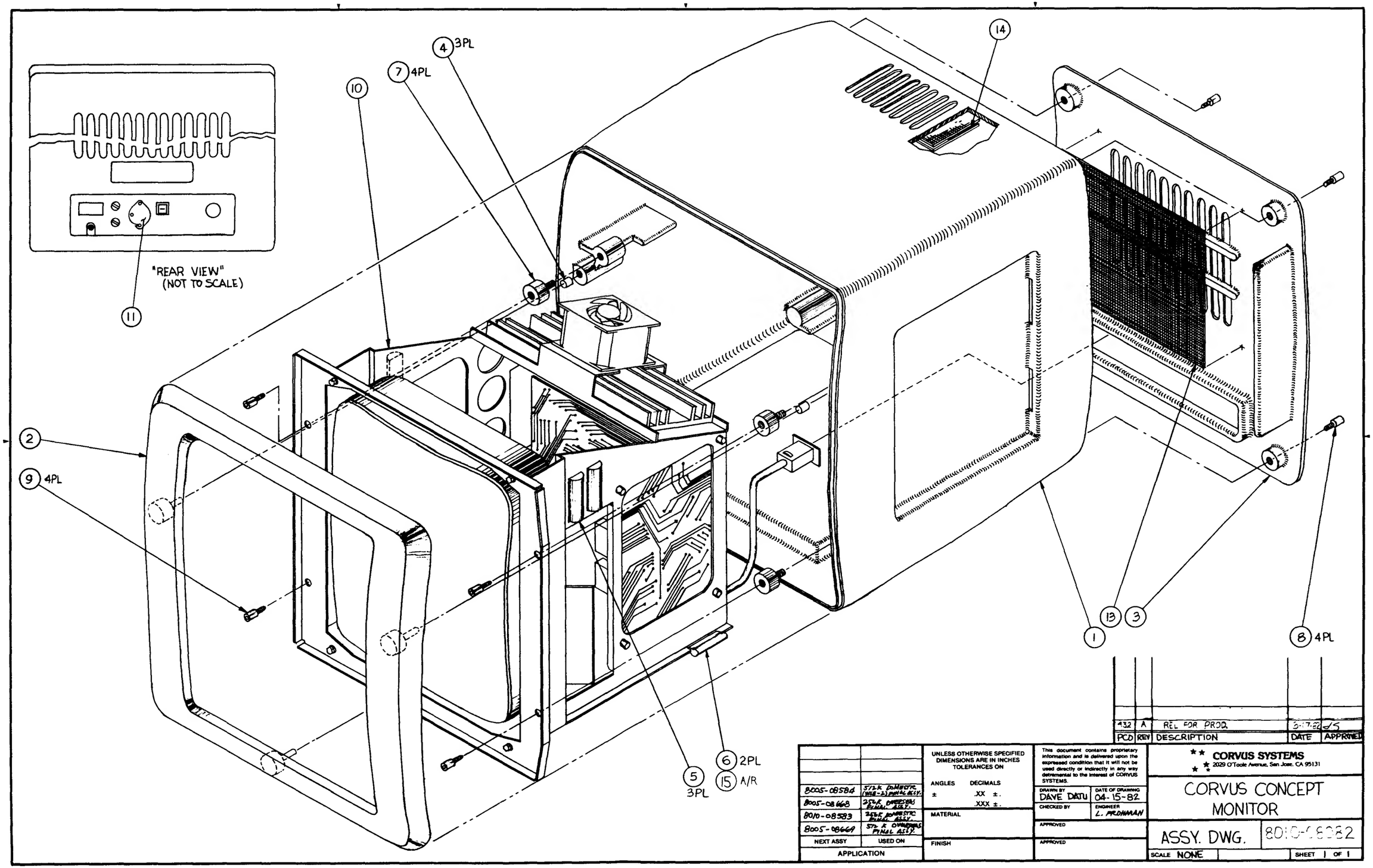
APPROVED

CORVUS SYSTEMS
2029 O'Toole Avenue, San Jose, CA 95131

CORVUS CONCEPT
512 KB MEMORY

ASSY. DWG. 8010-08546

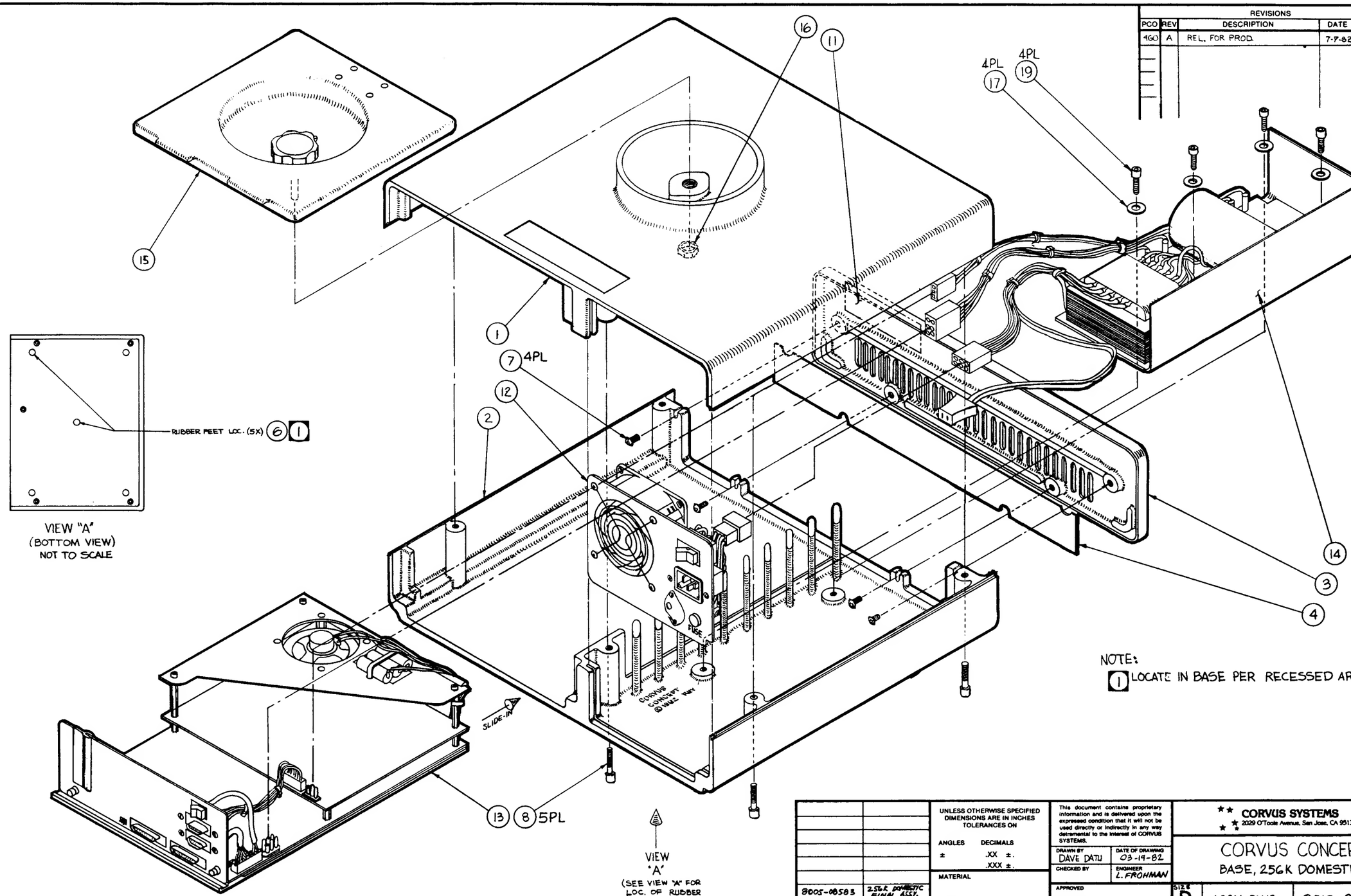
SCALE 3/2 — SHEET 1 OF 1



		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON	This document contains proprietary information and is delivered upon the expressed condition that it will not be used directly or indirectly in any way detrimental to the interest of CORVUS SYSTEMS.	★★ CORVUS SYSTEMS ★★ 2029 O'Toole Avenue, San Jose, CA 95131	
8005-08584	5¼" H. DOMESTIC (WSB-3) FINAL ASSY.	ANGLES ± DECIMALS .XX ±. .XXX ±.	DRAWN BY DAVE DATU	DATE OF DRAWING 04-15-82	CORVUS CONCEPT MONITOR
8005-08668	25" H. OVERSEAS FINAL ASSY.	MATERIAL	CHECKED BY	ENGINEER L. ARDHMAN	
8010-08583	25" H. DOMESTIC FINAL ASSY.		APPROVED		ASSY. DWG. 8010-08582
8005-08669	5¼" H. OVERSEAS FINAL ASSY.	FINISH	APPROVED		SCALE NONE SHEET 1 OF 1
NEXT ASSY	USED ON				
APPLICATION					

PCO	REV	DESCRIPTION	DATE	APPROVED
432	A	REL FOR PROD.	3-17-82	JS

REVISIONS				
PCO	REV	DESCRIPTION	DATE	APPROVED
960	A	REL. FOR PROD.	7-7-82	



NOTE:

1 LOCATE IN BASE PER RECESSED AREAS.

8005-08583	256K DOMESTIC FINAL ASSY.
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON
ANGLES ± DECIMALS .XX ± . .XXX ± .
MATERIAL
FINISH

DRAWN BY: DAVE DATU — DATE OF DRAWING: 03-19-82
CHECKED BY — ENGINEER: L. FROHMAN
APPROVED
APPROVED

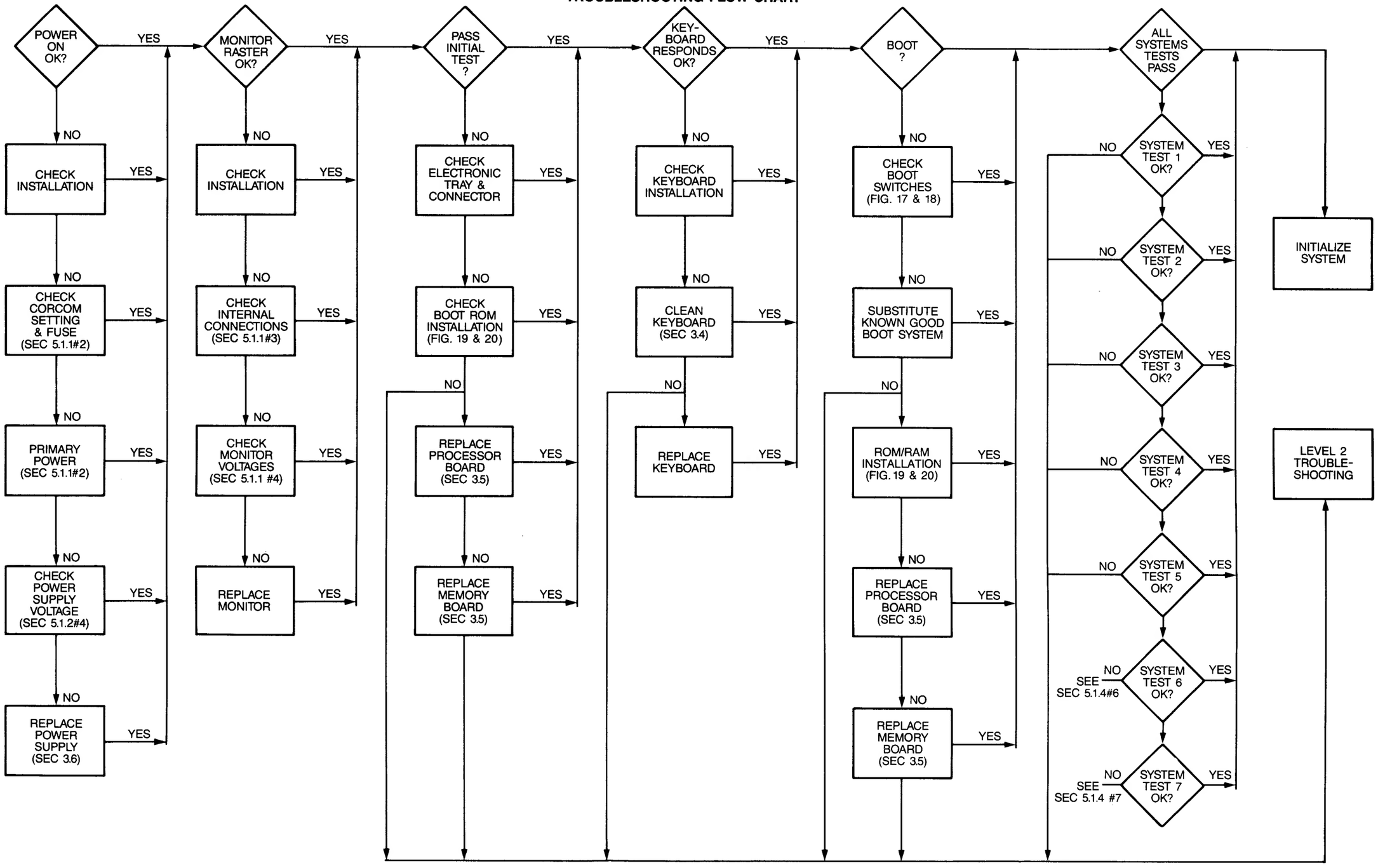
CORVUS SYSTEMS
2029 O'Toole Avenue, San Jose, CA 95131

CORVUS CONCEPT
BASE, 256K DOMESTIC

SIZE D — ASSY. DWG. 8010-08081
SCALE NONE — SHEET 1 OF 1

APPENDIX B
TROUBLESHOOTING FLOW CHART

LEVEL ONE
TROUBLESHOOTING FLOW CHART



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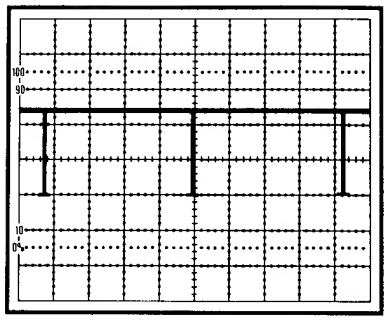
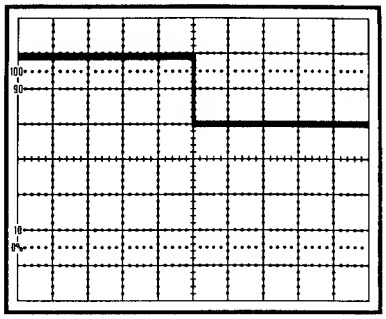
APPENDIX C-1
PROCESSOR BOARD
TEST POINT SIGNALS

TP 13 NOMNIT



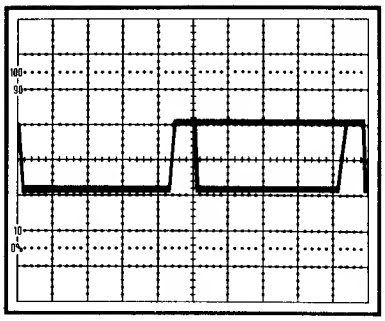
2V/DIV @ 2 ms

TP 14 HALT



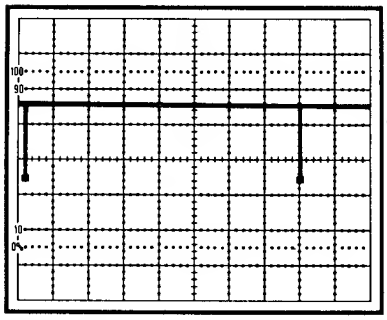
2V/DIV @ 2 us

TP 15 NWRITE



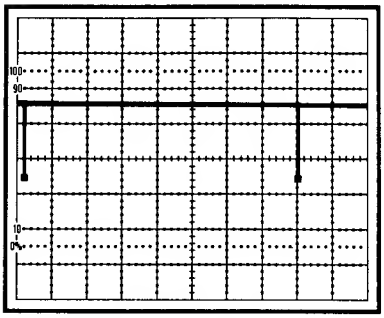
2V/DIV @ 2 us

TP 16 IPL1



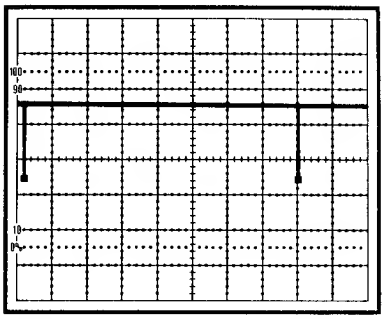
2V/DIV @ 10 ms

TP 17 IPL2



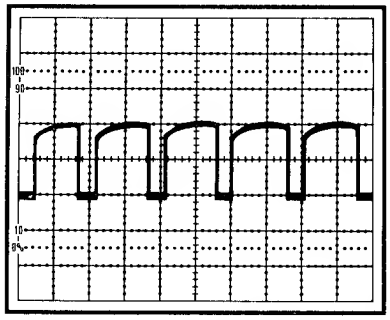
2V/DIV @ 10 ms

TP 18 IPL0



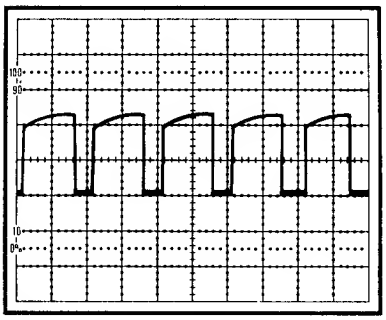
2V/DIV @ 10 ms

TP 19 DS



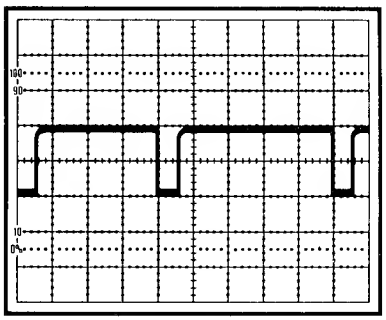
2V/DIV @ .5 us

TP 20 NDTACK



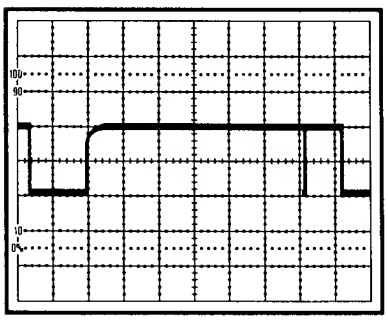
2V/DIV @ .5 us

TP 21 NSRO



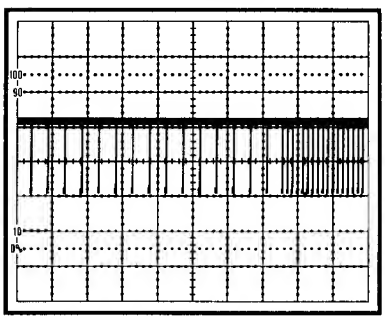
2V/DIV @ 2 us

TP 22 NDEVS



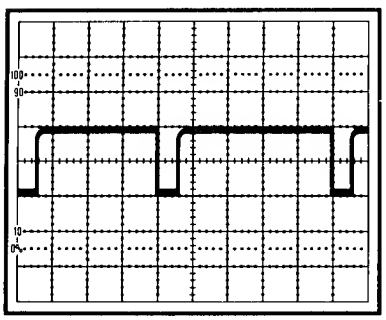
2V/DIV @ 1 us

TP 23 NKBD

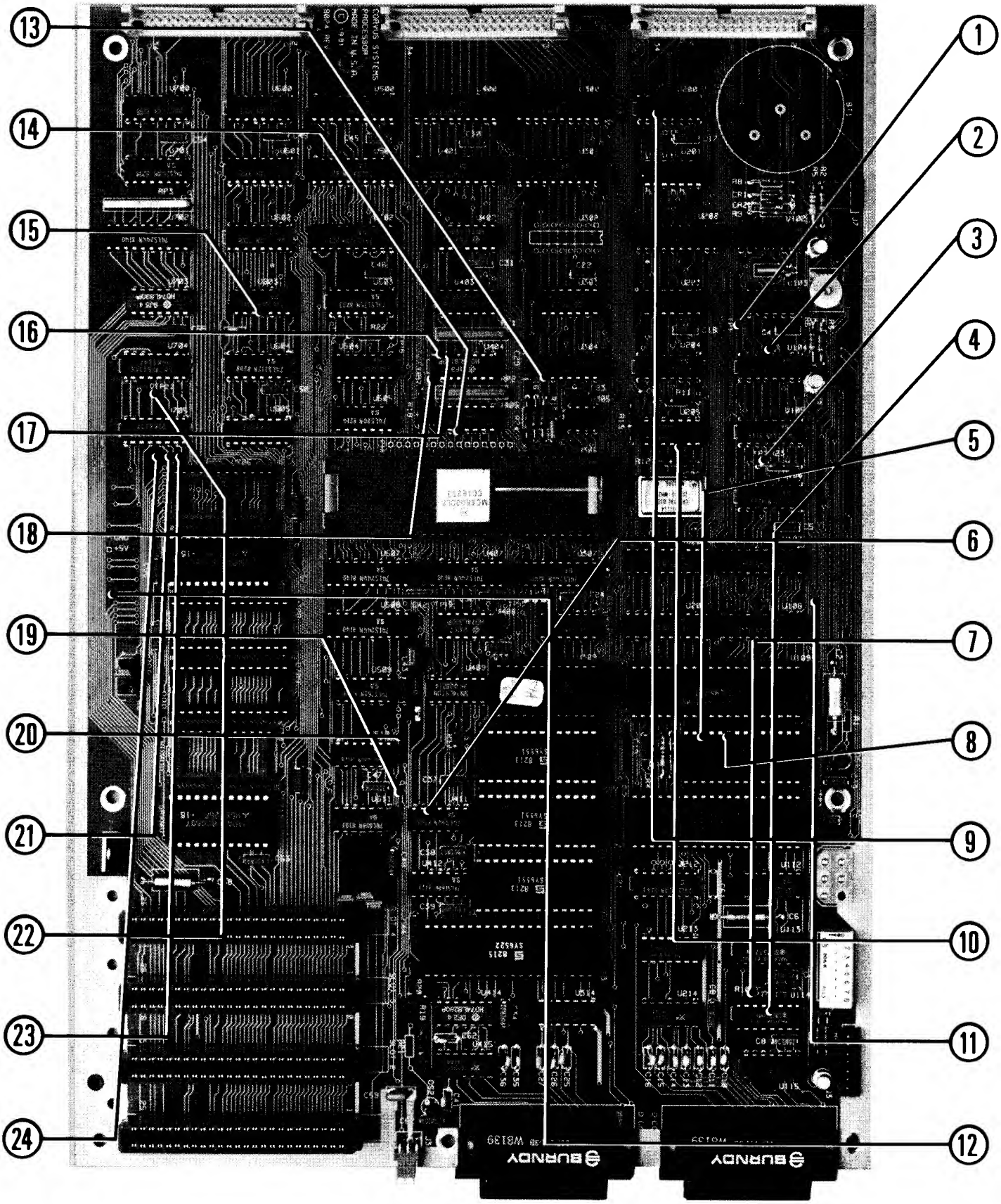


2V/DIV @ 1 ms

TD 24 NSRI



2V/DIV @ 2 us


1
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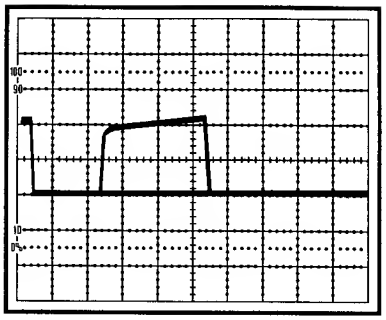
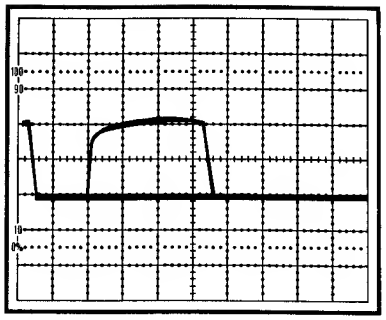
TP 1 DMAG02



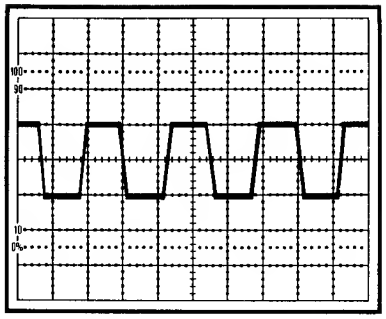
2V/DIV @ .2 us

TP 2 DMAEN



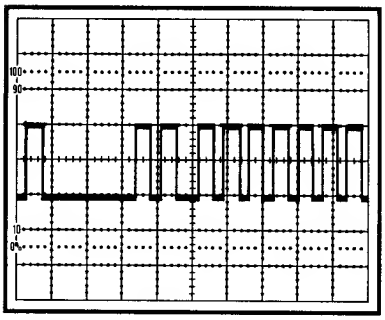
2V/DIV @ .2 us

TP 3 8M



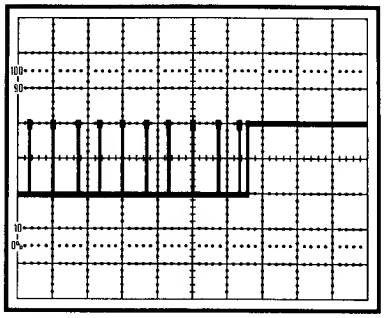
2V/DIV @ .05 us

TP 4 TXENA



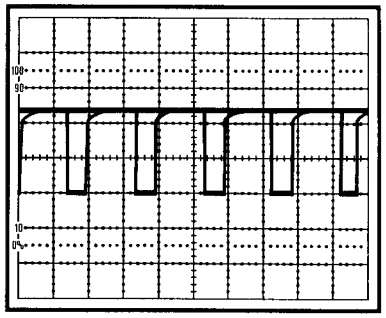
2V/DIV @ 2 ms

TP 5 IN/OUT



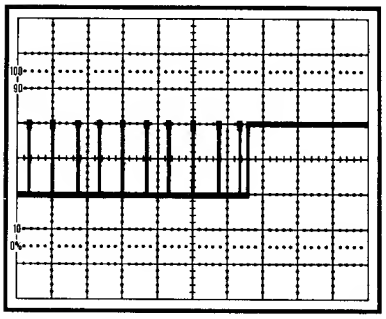
2V/DIV @ 2 us

TP 6 NTACK



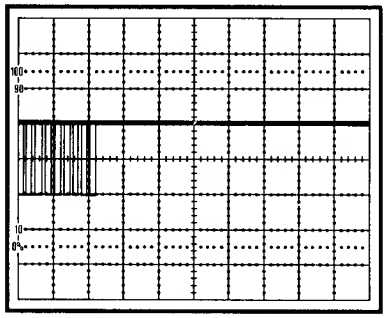
2V/DIV @ .5 us

TP 7 TXD



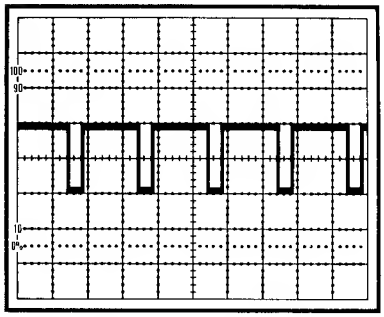
2V/DIV @ 2 us

TP 8 NCS



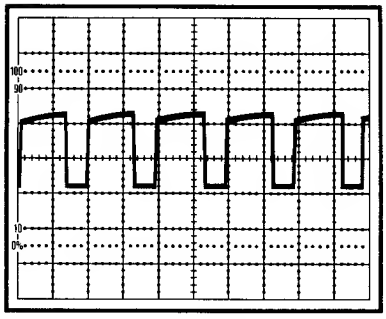
2V/DIV @ 5 ms

TP 9 RAMSEL



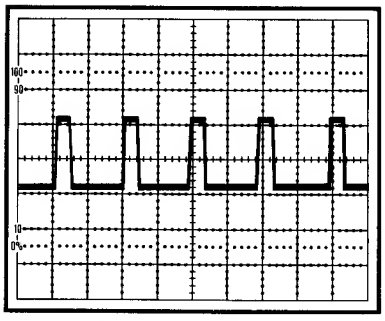
2V/DIV @ .5 us

TP 10 NRAMACK



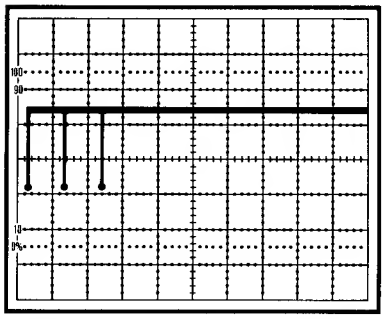
2V/DIV @ .5 us

TP 11 NAS



2V/DIV @ .5 us

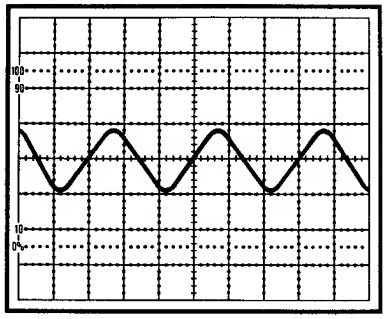
TP 12 NOMNI



2V/DIV @ .1 us

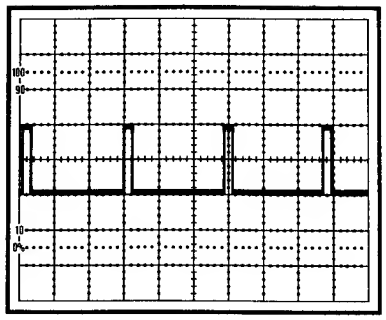
APPENDIX C-2
MEMORY BOARD
TEST POINT SIGNALS

MTP 1 16M



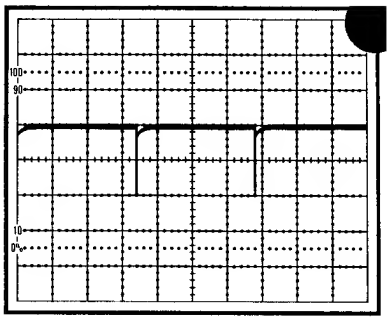
2V/DIV @ .02 us

MTP 2 HSYNC



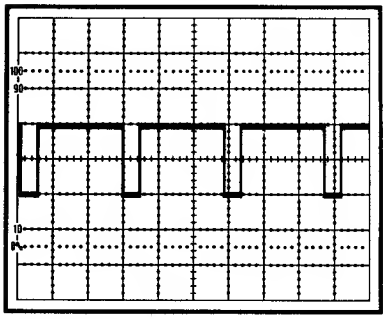
2V/DIVD @ 10 us

MTP 3 VSYNC



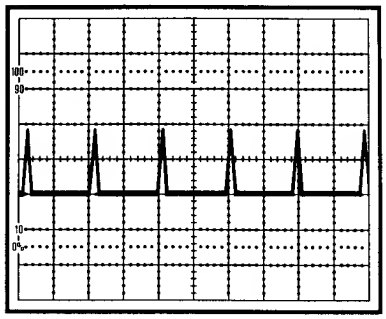
2V/DIV @ 5 ms

MTP 4 ENVID



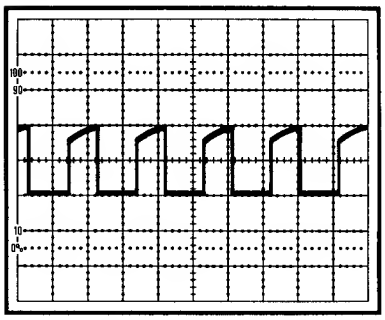
2V/DIV @ 10 us

MTP 5 LOADVID



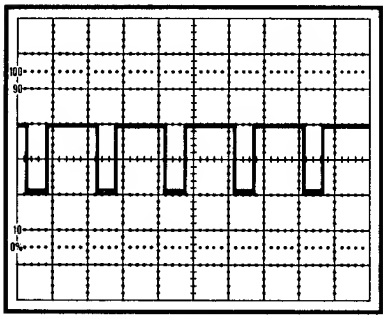
2V/DIV @ 10 us

MTP 6 NVIDTIME



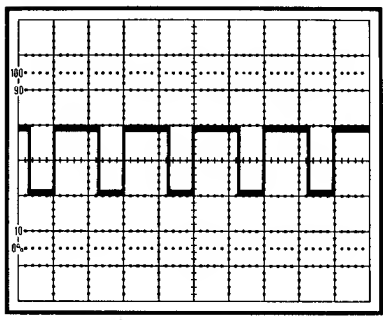
2V/DIV @ .5 us

MTP 7 MUX



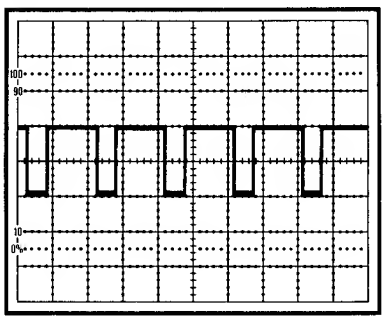
2V/DIV @ .5 us

MTP 8 NRASTIME



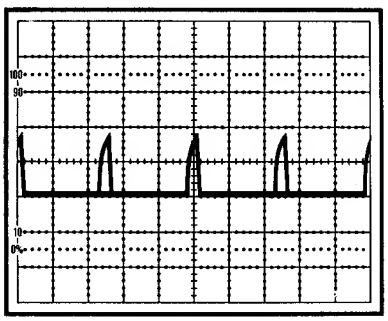
2V/DIV @ .5 us

MTP 9 NLASTIME



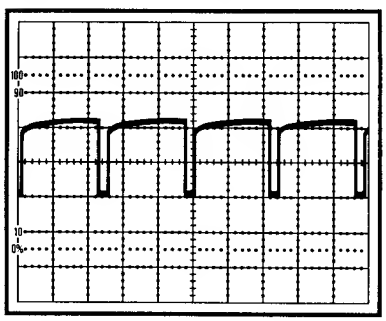
2V/DIV @ .5 ms

MTP 10 68K



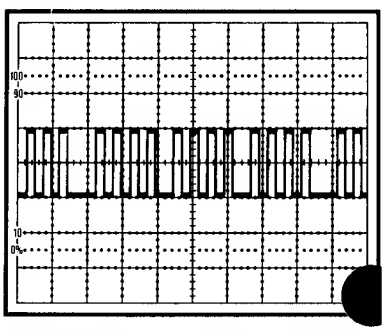
2V/DIV @ .2 us

MTP 11 N10L

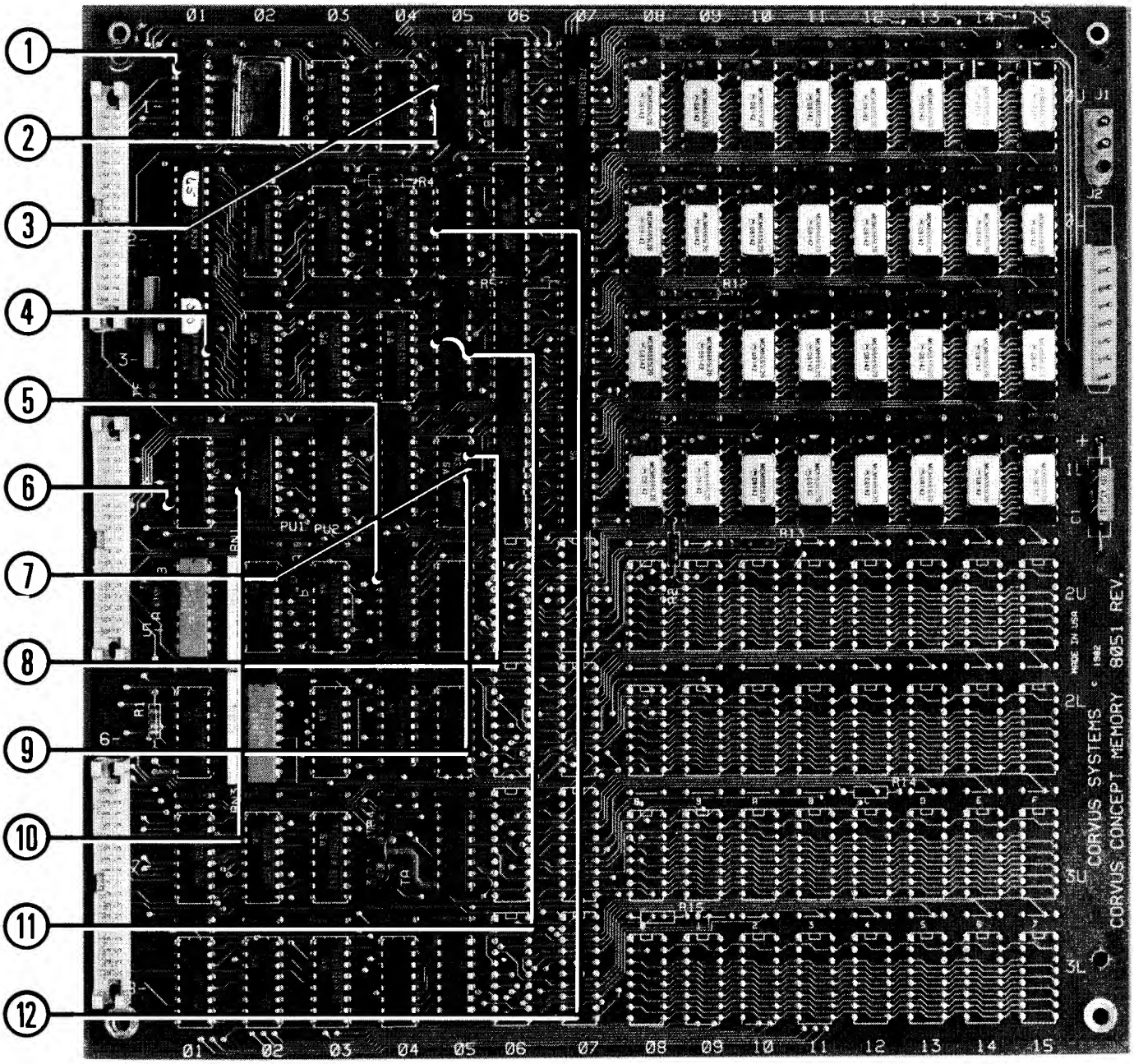


2V/DIV @ 2 us

MTP 12 LATCHRAM



2V/DIV @ 2 us


1
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12
CORVUS SYSTEMS © 1982 8051 REV.
CORVUS CONCEPT MEMORY

APPENDIX D
TIMING CHARTS

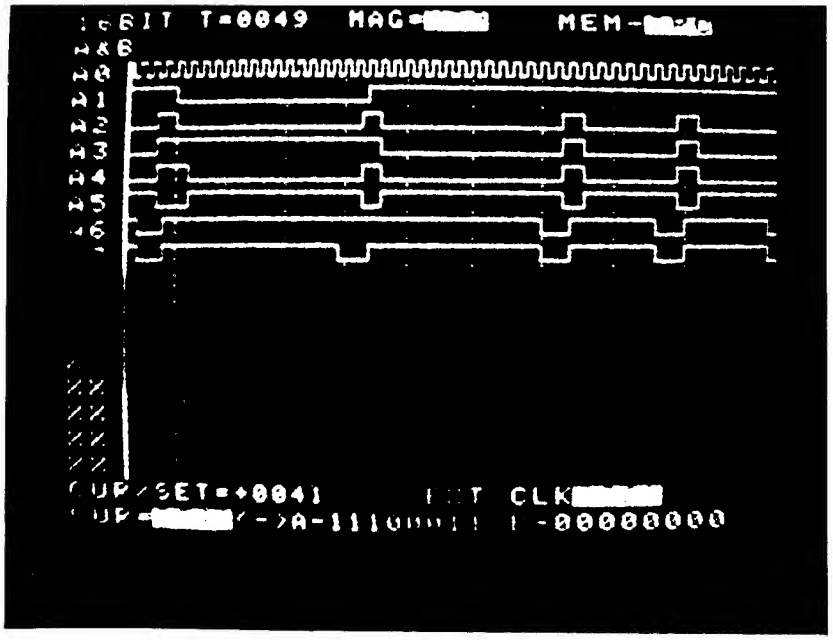
APPENDIX D
TIMING DIAGRAMS

The following charts require specific tests and routines to be executing. A dual trace oscilloscope is required on the following steps. The programs that are listed below are available from Corvus only to authorized Corvus Concept service dealers. It is recommended that backups be made of the diagnostic floppy. In instances where the 50 pin I/O slots are defective, a copy on a network system will be helpful. The following steps are to indicate timing relationships between key signals and not their waveshapes.

D.1 Processor Timing

Setup: MACSbug
Option: DM 80000
External Clock: 16 MHz
Trigger: NAS (U103-2)

Processor Timing Diagrams

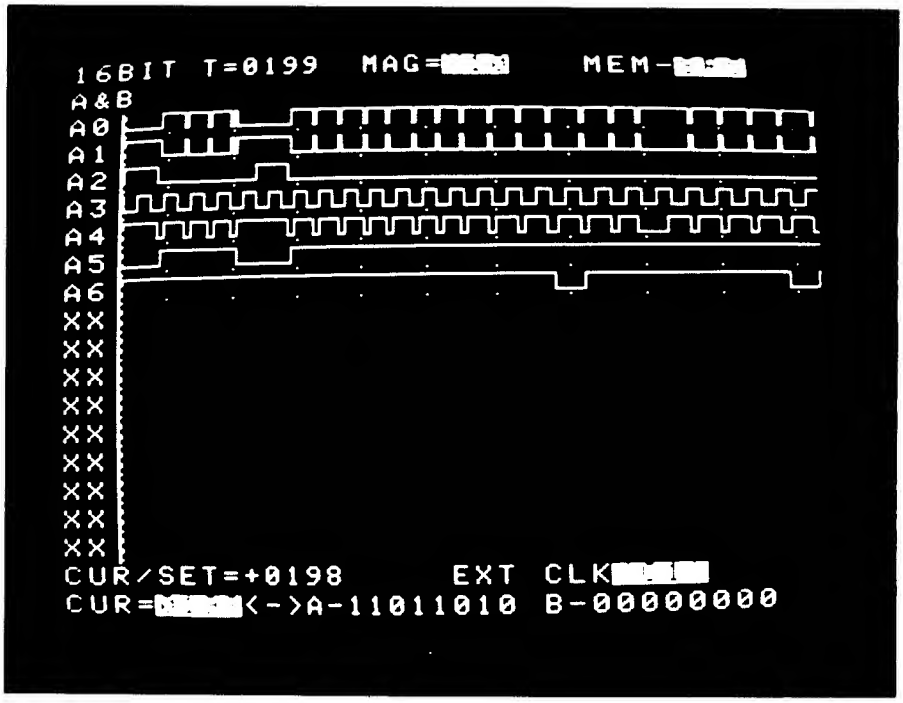


A0 — 8MHz — U103-6
A1 — NWRITE — U307-9
A2 — NAS — 307-14
A3 — NUDS — 307-7
A4 — NLDS — U307-12
A5 — DS — U308-8
A6 — NTACK — U411-5
A7 — NDTACK — U510-6

D.2 Local Drive Boot

Setup: Boot Local Drive
External Clock: 1 Mz
Trigger: NIO

Local Drive Boot Timing Diagram

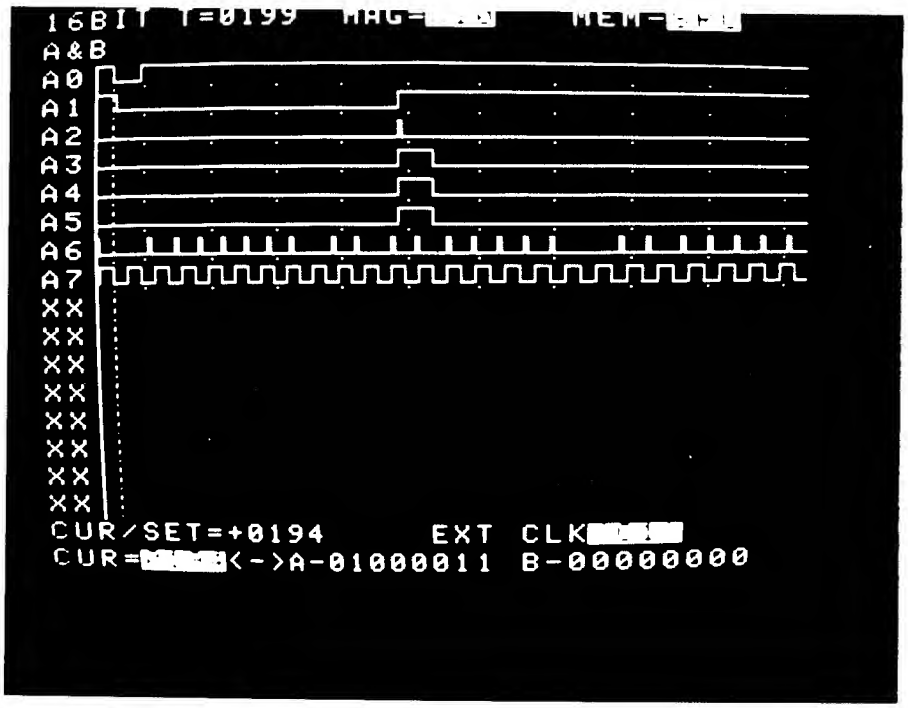


A0 — NIO — U605-44
A1 — IO — U604-33
A2 — IOGO — U604-5
A3 — IOACK — U605-3
A4 — NEVS — U605-15
A5 — NIO2 — U605-13
A6 — NDEV2 — U704-13
A7 — NIOSTB — U705-7

D.3 Omninet Signals

Setup: O Test
Option: Send Set
External Clock: 16 Mz
Trigger: NOMNI 3rd pass

Omninet Timing Diagram

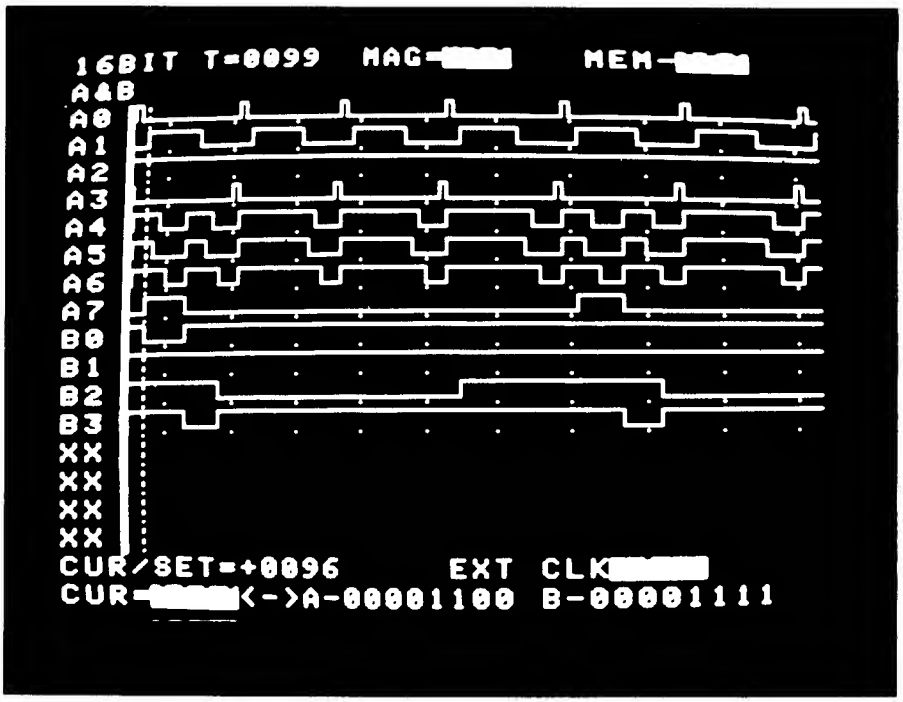


A0 — NOMNI — U109-32
A1 — READY — U109-311
A2 — DMAREQ — U109-34
A3 — DMAEN — U104-5
A4 — DMAGO2 — U104-9
A5 — RAMSEL — U203-8
A6 — 68KRAMSEL — U205-5
A7 — NRAMACK — U205-11

D.4 Ram Access Timing

Setup: MAGSbug
Optional Clock: DM 80000 or Location in Question
External Clock: 16 Mz
Trigger: LATCHRAM

Ram Access Timing Diagram



A0 — 68K — MU401-12
A1 — NVIDTIME — MU401-7
A2 — ENVID — MU301-15
A3 — LOADVID — MU504-2
A4 — MUX — MU405-14
A5 — NRASTIME — MU405-15
A6 — NCASTIME — MU405-13
A7 — LATCHRAM — MU205-4
B0 — NWU — MU305-3
B1 — NWL — MU305-11
B2 — RAMSEL — MU604-9
B3 — NRAMACK — MU504-4

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APPENDIX E-1
MACSBUG COMMANDS

APPENDIX E-1
MACSBUG COMMANDS

A detailed explanation of the features of MACSbug can be found in the Motorola MACSbug User's Guide. There are two mnemonics that will be used extensively:

- Set Memory (SM)
- Display Memory (DM)

The following sequence is an example of their use:

MACSBUG 2.0

```
*SM 80000 OF 5A AA 22 00 11      ; sm is the command to set memory.
                                 ; 80000 is the address in memory.
                                 ; OF 55 AA is the data to be written.

*DM 80000

80000   OF 5A AA 22 00 11 00 00 00 00 00 00 00 00 00 00
```

These two commands will aid in diagnosing a memory failure. For example:

```
                bank 1 (256k)
        bank 1  bank 3 (512k)

80000 OF 5A AA 22 00 11 00 00 00 00 00 00 00 00 00 00

        bank 0  bank 2 (512K)
                bank 0 (256K)
```

Each bank can then be divided into upper and lower bytes.

```
          OF          5A
      upper byte   lower byte
```

The byte can then be further divided into eight bits.

```
   0        F        5        A
 0000     1111     0101     1010
  /        /        /        /
it (F)  bit (8)  bit (7)  bit (0)
```

DM is the command to display memory. The computer will respond with the contents of the specified address plus the next sixteen locations.

This memory dump can be further divided down into segments.

APPENDIX E-2
MACSBUG ROUTINES

APPENDIX E-2
MACSBUG ROUTINES

The following routines require Motorola's 68000 monitor program MACSbug. This monitor program may be purchased from Corvus Systems. The following routines are here for examples and may be modified to fit specific needs. Upon entering MACSbug, memory must be set to the listed hexadecimal equivalents. A recommended memory starting location would be static RAM location $700.

TESTZERO

```
                                1*              ident       testzero
                                2* ;TEST ZERO LOAD ZERO FOREVER AT BANK ZERO LOCATION
                                3* ;                                                    $80000
0000    207C    0008    0000    4* test0        move. 1     #$80000, a0
0006    4280                    5*              clr. 1      d0
0008    3080                    6* test0x       move. w     d0, (a0)    ; moves zeros into $8000
000A    60FC                    7*              bra. s      test0x
                                8* ;
                                9* ; TEST ONE LOAD $FFFF FOREVER AT BANK ZERO LOCATION
                               10* ;                                                    $80000
000C    207C    0008    0000   11* test1        move. 1     #$80000, a0
0012    303C    FFFF           12*              move        #$ffff, d0
0016    3080                   13* test1x       move        d0, (a0)    ; moves $ffff into $80000
0018    60FC                   14*              bra. s      test1x
                               15* ;
                               16* ; TEST TWO AND THREE, SAME AS TEST ZERO AND ONE BUT
                               17* ;                                                    FOR BANK ONE
                               18* ; ----TEST TWO LOAD ZERO FOREVER AT LOCATION $80002
001A    207C    0008    0002   19* test2        move. 1     #$80002, a0
0020    4280                   20*              clr. 1      d0
0022    3080                   21* test2x       move. w     d0, (a0)    ; moves zeros into $80002
0024    60FC                   22*              bra. s      test2x
                               23* ;
                               24* ; --TEST THREE LOAD ZERO FOREVER AT LOCATION $80002
0026    207C    0008    0002   25* test3        move. 1     #$80002, a0
002C    303C    FFFF           26*              move        #$ffff, d0
0030    3080                   27* test3x       move        d0, (a0)    ; moves $ffff into $80002
0032    60FC                   28*              bra. s      test3x
                               29* ;
                               30* ; TEST FOUR FILLS $80000 TO END OF MEMORY WITH ZERO
0034    207C    0008    0000   31* test4        move. 1     #$80000, a0
003A    4280                   32*              clr. 1      d0
003C    30C0                   33* test4x       move. w     d0, (a0)+   ; moves zero into $80000
                               34* ;                                    and increments memory
003E    60FC                   35*              bra. s      test4x
                               36* ;
                               37* ; TEST FIVE FILLS $80000 TO END WITH $FFFF
0040    207C    0008    0000   38* test5        move. 1     #$80000, a0
0046    303C    FFFF           39*              move        #$ffff, d0
004A    30C0                   40* test5x       move. w     d0, (a0)+   ; moves $ffff into
                               41* ;                                                    all of memory
004C    60FC                   42*              bra. s      test5x
                               43* ;
```

```
                                    44* ; TEST SIX READ FROM LOCATION $80000 BANK ZERO
004E  207C  0008  0000    45* test6     move. 1   #$80000, a0
0054  3010                46* test6x    move. w   (a0), d0      ; reads from $80000 and
                          47* ;                                          writes data to d0
0056  60FC                48*           bra. s    test6x
                          49* ;
                          50* ; TEST SEVEN READS FROM BANK ONE AT LOCATION $80002
0058  207C  0008  0002    51* test7     move. 1   #$80002, a0
005E  3010                52* test7x    move. w   (a0), d0
0060  60FC                53*           bra. s    test7x
                          54* ;
                          55* ; TEST EIGHT WRITE DO TO $80000 AD READ IT BACK
0062  207C  0008  0000    56* test8     move. 1   #$80000, a0
0068  4280                57*           clr. 1    d0
006A  3080                58* test8x    move. w   d0, (a0)
006C  3210                59*           move. w   (a0), d1
006E  60FA                60*           bra. s    test8x
                          61* ;
                          62* ; TEST NINE WRITE ZERO TO BANK ONE AT LOCATION
                          63* ;   $80002 AND READ IT BACK
0070  207C  0008  0002    64* test9     move. 1   #$80002, a0
0076  4280                65*           clr. 1    d0
0078  3080                66* test9x    move. w   d0, (a0)
007A  3210                67*           move. w   (a0), d1
007C  60FA                68*           bra. s    test9x
                          69* ;
                          70* ; TEST TEN FILLS RAM WITH AN INCREMENTING PATTERN
007E  207C  0008  0000    71* test10    move. 1   #$80000, a0
0084  30C0                72* test10x   move      d0, (a0)+
0086  5240                73*           addq      #1, d0
0088  60FA                74*           bra. s    test10x
                          75* ;
                          76* ; TEST ELEVEN SEND DATACOMM ZERO
      00030F21            77* ddata0    equ       $30f21
      00030F23            78* dstat0    equ       $30f23
      00030F25            79* dcomm0    equ       $30f25
      00030F27            80* dcont0    equ       $30f27
      000000AB            81* commd0    equ       $ab
      00000037            82* contr0    equ       $37
      00000007            83* txready   equ       $07
008A  13FC  00AB  0003    84* test11    move. b   #commd0, dcomm0. 1
0090  0F25
0092  13FC  0037  0003    85*           move. b   #contr0, dcont0. 1
0098  0F27
009A  103C  0040          86*           move. b   #'@', d0
009E  0839  0007  0003    87* test11x   btst      #txready, dstat0. 1
00A4  0F23
00A6  66F6                88*           bne. s    test11x
00A8  13C0  0003  0F21    89*           move. b   d0, ddata0. 1
00AE  60EE                90*           bra. s    test11x
```

```
                                        92* ; TEST TWELVE SENDS FROM DATACOMM ONE
        00030F41                        93* ddata1      equ     $30F41
        00030F43                        94* dstat1      equ     $30f43
        00030F45                        95* dcomm1      equ     $30f45
        00030F47                        96* dcont1      equ     $30f47
        000000AB                        97* commd1      equ     $ab
        00000037                        98* contr1      equ     $37
00B0    13FC    00AB    0003            99* test12      move. b #commd1, dcomm1. 1
00B6    0F45
00B8    13FC    0037    0003            100*            move. b #contr1, dcont1. 1
00BE    0F47
00C0    103C    0040                    101*            move. b #'@', d0
00C4    0839    0007    0003            102* test12x     btst    #txready, dstat1. 1
00CA    0F43
00CC    66F6                            103*            bne. s  test12x
00CE    13C0    0003    0F41            104*            move. b d0, ddata1. 1
00D4    60EE                            105*            bra. s  test12x
                                        106*            end
COMMDO          000000AB        DDATA0          00030F21        TEST10X         000084+
COMMD1          000000AB        DDATA1          00030F41        TEST11          00008A+
CONTR0          00000037        DSTAT0          00030F23        TEST11X         00009E+
CONTR1          00000037        DSTAT1          00030F43        TEST12          0000B0+
DCOMM0          00030F25        TEST0             000000+       TEST12X         0000C4+
DCOMM1          00030F45        TEST0X            000008+       TEST1X          000016+
DCONT0          00030F27        TEST1             00000C+       TEST2           00001A+
DCONT1          00030F47        TEST10            00007E+       TEST2X          000022+
TEST3             000026+       TEST7             000058+
TEST3X            000030+       TEST7X            00005E+
TEST4             000034+       TEST8             000062+
TEST4X            00003C+       TEST8X            00006A+
TEST5             000040+       TEST9             000070+
TEST5X            00004A+       TEST9X            000078+
TEST6             00004E+       TXREADY         00000007
TEST6X            000054+
```

APPENDIX E-3
SELF-TEST ROUTINES

APPENDIX E-3
SELF-TEST ROUTINES

The following routines are derived from the Concept's Self Test. There are some differences between these routines and that of the Self Test, however they are functionally identical.

```
                                    1*              ident     ramtest
0000                                2*  start       org       $0
      00000000                      3*  rambase     equ       $0000
      00000700                      4*  srambeg     equ       rambase+$700
      00000F00                      5*  sramend     equ       srambeg+$800
      00080000                      6*  dspbase     equ       $80000
      0000E000                      7*  dsplen      equ       $0e000
      0008E000                      8*  dspend      equ       dspbase+dsplen
      00000400                      9*  ramxbug     equ       rambase+$400
      00010000                     10*  rombase     equ       $10000
      00002000                     11*  romlen      equ       $2000
      00012000                     12*  romend      equ       rombase+romlen
                                   13*  ;
                                   14*  ; SRAM TEST WALKBIT AND MARCHING
0000  4DFA  0006+                  15*              lea       ramtst1, a6     ; loads starting
                                                                              address into a6
0004  6100  0130                   16*  max         bsr       trapp           ; jumps out
                                                                              to MACSbug
0008  207C  0000  0700             17*  Ramtst1     move. 1   #srambeg, a0
000E  6100  006E                   18*              bsr       walkbit
0012  660C                         19*              bne. s    rt1err
0014  227C  0000  0F00             20*              move. 1   #sramend, a1
001A  6100  0094                   21*              bsr       march
001E  670A                         22*              beq. s    ramtst2
0020  2C3C  0000  0001             23*  rt1err      move. 1   #$0001, d6
0026  6100  010E                   24*              bsr       trapp
                                   25*  ;
002A  207C  0008  E000             26*  ramtst2     move. 1   #dspend, a0
0030  6100  004C                   27*              bsr       walkbit
0034  660A                         28*              bne. s    rt2err
0036  6100  00C4                   29*              bsr       ramsize
003A  6100  0074                   30*              bsr       march
003E  670A                         31*              beq. s    memtest
0040  2C3C  0000  0002             32*  rt2err      move. 1   #$0002, d6
0046  6100  00EE                   33*              bsr       trapp
                                   34*  ;
004A  6100  0090                   35*  memtest     bsr       inctest
004E  670A                         36*              beq. s    memclr
0050  2C3C  0000  0003             37*              move. 1   #$0003, d6
0056  6100  00DE                   38*              bsr       trapp
                                   39*  ;
005A  207C  0000  0F00             40*  memclr      move. 1   #sramend, a0
0060  227C  0000  0EFE             41*              move. 1   #sramend-2, a1
0066  6100  00BE                   42*              bsr       zeroram
006A  2A3C  0000  0001             43*              move. 1   #01, d5
0070  207C  0008  0000             44*              move. 1   #dspbase, a0
```

```
0076  6100  0084          45*            bsr      ramsize
007A  6100  00AA          46*            bsr      zeroram
                          47* ;
007E  2448                48* walkbit    move. 1  a0, a2
0080  2248                49*            move. 1  a0, a1
0082  D3FC  0000  0010    50*            adda. 1  #$10, a1
0088  303C  FFFE          51* wb1        move. w  #$fffe, d0
008C  3480                52* wb2        move. w  d0, (a2)
008E  B052                53*            cmp. w   (a2), d0
0090  661C                54*            bne. s   wberr
0092  E358                55*            rol      #1, d0
0094  65F6                56*            bcs. s   wb2
0096  303C  0001          57*            move. w  #$0001, d0
009A  3480                58* wb3        move. w  d0, (a2)
009C  B052                59*            cmp. w   (a2), d0
009E  660E                60*            bne. s   wberr
00A0  E340                61*            as1      #1, d0
00A2  64F6                62*            bcc. s   wb3
00A4  D5FC  0000  0002    63*            adda. 1  #2, a2
00AA  B5C9                64*            cmpa. 1  a1, a2
00AC  6DDA                65*            blt. s   wb1
00AE  4E75                66* wberr      rts
                          67* ;
00B0  2448                68* march      move. 1  a0, a2
00B2  4280                69*            clr. 1   d0
00B4  34C0                70* mr1        move. w  d0, (a2)+
00B6  B5C9                71*            cmpa. 1  a1, a2
00B8  66FA                72*            bne. s   mr1
00BA  3400                73*            move. w  d0, d2
00BC  4642                74*            not. w   d2
00BE  3222                75* mr2        move. w  -(a2), d1
00C0  B240                76*            cmp. w   d0, d1
00C2  6616                77*            bne. s   mrerr
00C4  3482                78*            move. w  d2, (a2)
00C6  B5C8                79*            cmpa. 1  a0, a2
00C8  66F4                80*            bne. s   mr2
00CA  3002                81*            move. w  d2, d0
00CC  4642                82*            not. w   d2
00CE  3212                83* mr3        move. w  (a2), d1
00D0  B240                84*            cmp. w   d0, d1
00D2  6606                85*            bne. s   mrerr
00D4  34C2                86*            move. w  d2, (a2)+
00D6  B5C9                87*            cmpa. 1  a1, a2
00D8  66F4                88*            bne. s   mr3
00DA  4E75                89* mrerr       rts
                          90* ;
00DC  2448                91* inctest    move. 1  a0, a2
00DE  323C  0101          92*            move. w  #$101, d1
00E2  34C1                93* ito1       move. w  d1, (a2)+
00E4  E359                94*            rol. w   #1, d1
00E6  B5C9                95*            cmpa. 1  a1, a2
00E8  6DF8                96*            blt. s   ito1
00EA  2448                97*            move. 1  a0, a2
```

```
00EC  323C  0101          98*           move. w   #$101, d1
00F0  B25A                99* ito2      cmp. w    (a2)+, d1
00F2  6606               100*           bne. s    it99
00F4  E359               101*           rol. w    #1, d1
00F6  B5C9               102*           cmpa. 1   a1, a2
00F8  6DF6               103*           blt. s    ito2
00FA  4E75               104* it99      rts
                         105* ;
00FC  227C  0009  0000   106* ramsize   move. 1   #$90000, a1
0102  0C97  0001  2000   107*           cmpi. 1   #romend, (sp)
0108  6E1A              108*           bgt. s    ramsiz9
010A  23FC  000F  FFFC   109* ramsiz1   move. 1   #$ffffc, $ffffc. 1
0110  000F  FFFC
0114  23FC  000B  FFFC   110*           move. 1   #$bfffc, $bfffc. 1
011A  000B  FFFC
011E  2279  000F  FFFC   111*           move. 1   $ffffc. 1, a1
0124  4E75               112* ramsiz9   rts
                         113* ;
0126  4298               114* zeroram   clr. 1    (a0)+
0128  B1C9               115*           cmpa. 1   a1, a0
012A  6FFA               116*           ble. s    zeroram
012C  BABC  0000  0001   117*           cmp. 1    #01, d5
0132  6702               118*           beq. s    trapp
0134  4E75               119*           rts
0136  4E4F               120* trapp     trap      #15
0138  0000               121*           data. w   0
013A  4E75               122*           rts
      00000004+          123*           end       max
```

```
DSPBASE   00080000   MAX       000004+   RAMSIZ1   00010A+
DSPEND    0008E000   MEMCLR    00005A+   RAMSIZ9   000124+
DSPLEN    0000E000   MEMTEST   00004A+   RAMSIZE   0000FC+
INCTEST    0000DC+   MR1        0000B4+   RAMTST1    000008+
IT99       0000FA+   MR2        0000BE+   RAMTST2    00002A+
IT01       0000E2+   MR3        0000CE+   RAMXBUG   00000400
IT02       0000F0+   MRERR      0000DA+   ROMBASE   00010000
MARCH      0000B0+   RAMBASE   00000000   ROMEND    00012000
ROMLEN    00002000   WB1        000088+
RT1ERR     000020+   WB2        00008C+
RT2ERR     000040+   WB3        00009A+
SRAMBEG   00000700   WBERR      0000AE+
SRAMEND   00000F00   ZERORAM    000126+
START      000000+
TRAPP      000136+
WALKBIT    00007E+
```

APPENDIX F-1
GENERAL MEMORY AND I/O MAPS

APPENDIX F-1
GENERAL MEMORY AND I/O MAPS

The following is a Memory and I/O Map of the Corvus Concept. Concept uses memory from 0 to $0FFFFF. I/O is in the range $030000 to $03FFFF. In the boxes are recommended addresses. "x" means "don't care." All addresses are hexadecimal. Actual addresses are shown, with possible alternate addresses in parentheses.

Static RAM	ROM 0	ROM 1	I/O
000008- 000FFF (000008- 00FFFF)	000000- 000007 010000- 011FFF (-01FFFF)	(020000- 02FFFF)	030000- 03FFFF

Dynamic RAM
080000-0FFFFF

\# NOTE: address bits 12, 13, 14, 15 = X
: addresses must be odd

DEVS I/O slot registers	IO1 ROM *	IO2 ROM *	IO3 ROM *	IO4 ROM *	SLOT STAT	CALENDAR R/W	I/O PORTS RS 232 Keys Etc.
0300xx- 0301xx	302xx 303xx	304xx 305xx	306xx 307xx	308 309xx	30Axx 30Bxx	030Cxx- 030Dxx	030Exx- 030Fxx

* see I/O ROM equivalences below

BIT	0	1	2	3	4	5	6	7
	NNMI	NNMI	NNMI	NNMI	NIRQ	NIRQ	NIRQ	NIRQ
SLOT	1	2	3	4	1	2	3	4

When an I/O slot NMI or IRQ interrupt occurs:

1. SlotINT causes an interrupt
2. Slotstat is read to find out which slot interrupted and whether it was an NMI or IRQ.

I/O SLOT DMA is not supported.

Key-Board	Dcomm 1	Dcomm 2	VIA	Calendar ALTMAP	OMNINET Strobe	OMNINET Interrupt Off	IOSTRB
			30F6x	Volume			
30Fxx	30F2x	30F4x	30F7x	30F8x	30FAx	030FCx	039FFF

APPENDIX F-2
ROM MAPPING OF I/O SLOTS

APPENDIX F-2
ROM MAPPING OF I/O SLOTS

To compare the address of a Corvus interface card when plugged in a Concept or an Apple II™ use this table.

The initial $C of APPLE is replaced by a $30. The lower three nibbles shifted left and 1 added.

Concept	Apple II™	I/O SLOT
$30201 $30203 $30205 $30207 . . $303FF	$C100 $C101 $C102 $C103 . . $C1FF	1
$30401 $30403 . $305FF	$C200 $C201 . $C2FF	2
$30601 . $307FF	$C300 . $C3FF	3
$30801 . $309FF	$C400 . $C4FF	4
$39FE1- $39FFF	$CFF0 $CFFF	IOSTRB

IOSTRB is only available in 16 locations.

Note that the 6502 code will not execute on a 68000. However the ROM ID and various tables may be useful. Drivers must be written in 68000 code and included in the operating system or attached using the INSTALL command. The 68000 code can be generated by Pascal or FORTRAN compilers as well as by the 68000 Assembler.

APPENDIX F-3
VIA GENERAL PURPOSE I/O PORT
(SYNERTEK 6522)

APPENDIX F-3
VIA GENERAL PURPOSE I/O PORT
(SYNERTEK 6522)

$30F61	ORB, IRB	Output register B, Input register B
$30F63	ORA, IRA	Output register A, Input register A handshake
$30F65	DDRB	Data direction register B (0 = in, 1 = out)
$30F67	DDRA	Data direction register A (0 = in, 1 = out)
$30F69	T1L-L, T1C-L	Timer 1 latch low byte, write latch, read counter
$30F6B	T1L-H	Timer 1 latch high byte
$30F6D	T1L-L	
$30F6F	T1L-H	
$30F71	T2L-L, T2C-L	
$30F73	T2C-H	
$30F75	SR	Shift Register
$30F77	ACR	Auxiliary Control Register
$30F79	PCR	Peripheral Control Register
$30F7B	IFR	Interrupt Control Register
$30F7D	IER	Interrupt Enable Register
$30F7F	ORA	Output register A, Input register A, no handshake

Port A -- DDRA (30F67) to preset to 80
ORA (30F7F) to read/write

0	Ready (OMNINET)		Input
1	Clear to send	DC0	Input
2	Clear to send	DC1	Input
3	Dataset ready	DC0	Input
4	Dataset ready	DC1	Input
5	Data carrier detect	DC0	Input
6	Data carrier detect	DC1	Input
7	IOX exclusive OR of above signals for interrupt		Output

Port B -- DDRB (30F65) preset to 37
ORB (30F61) to read/write

0	Video off		Output
1	Video address 17		Output
2	Video address 18		Output
3	Horizontal/vertical switch		Input
4	CH Rate select	DC0	Output
5	CH Rate select	DC1	Output
6	Boot switch 0		Input
7	Boot switch 1		Input

Note: The inputs are used in non-latching mode.
The bell speaker is controlled by the timer 2 and shift register.
The interrupt timer is timer 1.
For more detail see the Synertek 6522 application notes and handbook.

APPENDIX F-4
OMNINET

APPENDIX F-4
OMNINET

$30FA1-$30FBF	Transporter register
$30FC1-$30FDF	Reset OMNINET interrupt

For OMNINET operation refer to the OMNINET user's guide.

APPENDIX F-5
CLOCK/CALENDAR/ALTMAP/VOLUME

APPENDIX F-5

CLOCK/CALENDAR/ALTMAP/VOLUME

$030F81

The clock/calendar is a CMOS device with 'awkward' timing. The registers of the clock/calendar are addressed by data at $030F81. Data bits 0-3 are the register address. Bit 4 is the chip enable. Bits 5, 6 and 7 must be 0. Firstly the address must be written with the chip enable = 1. Then the address must be rewritten with the chip enable = 0. Thirdly the register read or write is performed at address $030C01. Finally $10 is written to $030F81 to deselect the chip. The data to or from the chip is on bits 0 to 3.

Bit 5 is the volume control for the bell. A zero must be written to bit whenever this register is written to, except when a quiet bell is sound. When the quiet bell has stopped sounding, a zero must again be written to this bit.

Bit 6 selects between the Concept memory mapping and an alternate Memory mapping. Whenever this register is written to, this bit must be set to zero.

APPENDIX F-6
DATA COMMUNICATION AND KEYBOARD REGISTERS

APPENDIX F-6
DATA COMMUNICATION AND KEYBOARD REGISTERS

The keyboard and Data Com use a 6551 UART from Synertek or Rockwell. For Data Com (and keyboard) the following relations are needed:

Register	Keyboard	Data Com 1	Data Com 2
Data	$030F01	$030F21	$030F61
Status	$030F03	$0303F23	$030F43
Command	$030F05	$030F25	$030F45
Control	$030F07	$030F27	$030F47

Command Register Bits

7	6	5	4	3	2	1	0	
x	x	0	x	x	x	x	x	no parity transmitted or received, no check
0	0	1	x	x	x	x	x	Odd parity transmitted and received
0	1	1	x	x	x	x	x	Even parity transmitted and received
1	0	1	x	x	x	x	x	Mark parity transmitted, no parity check
1	1	1	x	x	x	x	x	Space parity transmitted, no parity check
x	x	x	0	x	x	x	x	Normal transmit, receive (no echo)
x	x	x	1	x	x	x	x	Echo mode (received data is retransmitted)
x	x	x	x	0	0	x	x	Tx INT disabled, RTS off, Transmitter off
x	x	x	x	0	1	x	x	Tx INT enabled, RTS on, Transmitter on
x	x	x	x	1	0	x	x	Tx INT disabled, RTS on, Transmitter on
x	x	x	x	1	1	x	x	Tx INT disabled, RTS on, Transmit BREAK
x	x	x	x	x	x	0	x	IRQ interrupt enabled from bit 3 of status
x	x	x	x	x	x	1	x	IRQ interrupt disabled
x	x	x	x	x	x	x	0	Disable receiver, disable all interrupts
x	x	x	x	x	x	x	1	Enable receiver, enable all interrupts

Control Register Bits (7 6 5 4)

7	6	5	4	
0	x	x	x	One stop bit
1	x	x	x	2 stop bits on 7 bit words, 1 stop bit on 8 bit words
x	0	0	x	8 bit word length
x	0	1	x	7 bit word length
x	1	0	x	6 bit word length
x	1	1	x	5 bit word length

Control Register Bits (3 2 1 0)

0	16x external clock		8	1200	Baud
1	50	Baud	9	1800	Baud
2	75	Baud	A	2400	Baud
3	109.92	Baud	B	3600	Baud
4	134.58	Baud	C	4800	Baud
5	150	Baud	D	7200	Baud
6	300	Baud	E	9600	Baud
7	600	Baud	F	19200	Baud

Status Register Bits

Bit	Value		
0	0	No parity error	self clearing
	1	Parity error	
1	0	No Framing error	self clearing
	1	Overrun	
	1	Receive register full	(cleared by read data)
4	0	Transmit register full	(not ready for new data)
	1	Transmit register empty	(cleared by write data)
5	0	DCD low	(hard-wired low)
	1	DCD high	
6	0	DSR low	(hard-wired low)
	1	DSR high	
7	0	No interrupt request	
	1	Interrupt request	

Note: Writing to the status register resets status bit 2

Interrupt priority

7	Non maskable interrupt	not installed
6	Keyboard	
5	Timer	
4	Data Com 0	
3	OMNINET	
2	Data Com 1	
1	Data Com control/Apple slots	
0	Normal (no interrupt)	

When an interrupt occurs, the priority is automatically raised to the level of that interrupt, preventing further interrupts of the same priority or below. A return-from-interrupt restores the priority at the time of the interrupt. Most interrupts are self clearing; that is the reading of the status of the resource clears the interrupt. OMNINET interrupts must be cleared by accessing $030FC1 (NOMOFF). Data Com control line interrupts must be cleared by complementing bit 7 of VIA port A.

Memory Mapper Equivalents (PROM addresses and data) Signetics 82S181

Device pin	22	23	1	2	3	4	5	6	7	8			
Device Address	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0			
Concept BUS name	N ZERO 0	N SUPV X	N AS 0	A* 22 0	A 16 0	A 17 0	** 0	A 19 0	A 20	A 21	HEX ADDRESS	RESOURCE	DDDDDDDD 76543210
	1	X	0	0	0	0	0	0	0	0	000, 100	ROM0	01111110
	X	X	0	0	1	0	0	0	0	0	000, 100	ROM0	01111110 7E
									0	0	200, 300	SRAM	11111011 FB
	X	X	0	0	0	1	0	0	0	0	020, 120 220, 320	ROM0	01111110 7E
	X	X	0	0	1	1	0	0	0	0	010, 110 210, 310	ROM1	11111101 FD
	X	X	0	0	X	X	0	1	0	0	030, 130 230, 330	I/O	11011111 DF
									0	0	X04, X14 X24, X34 X84, X94 XA4, XB4	DRAM	11110111 F7

Here X is 0 or 1

Here x can be 0, 1, 2, 3

N NNNNNN
C IRRSRR
Y OAAROO

all other locations should be programmed to 7E

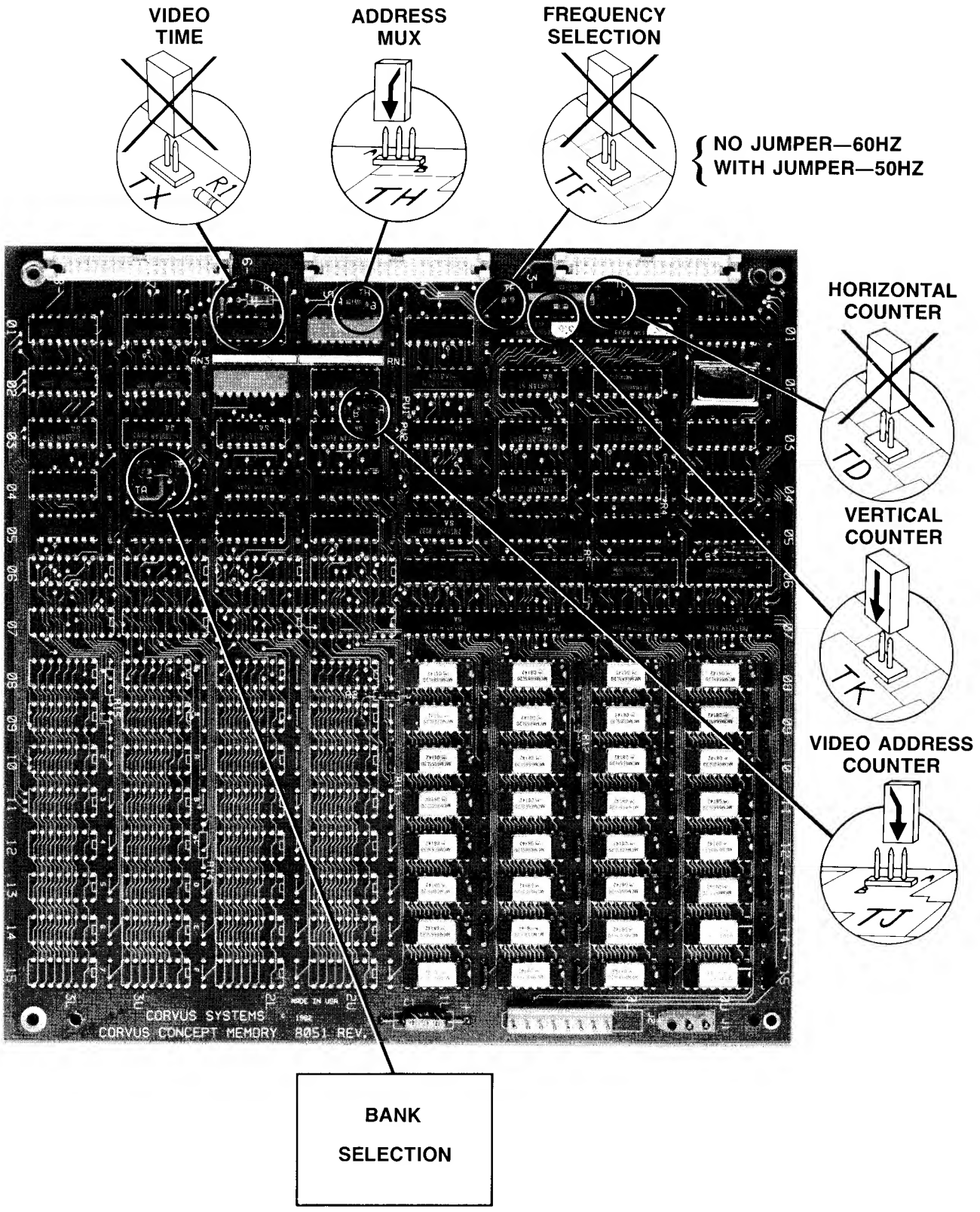
C MMAMM
L 10M10

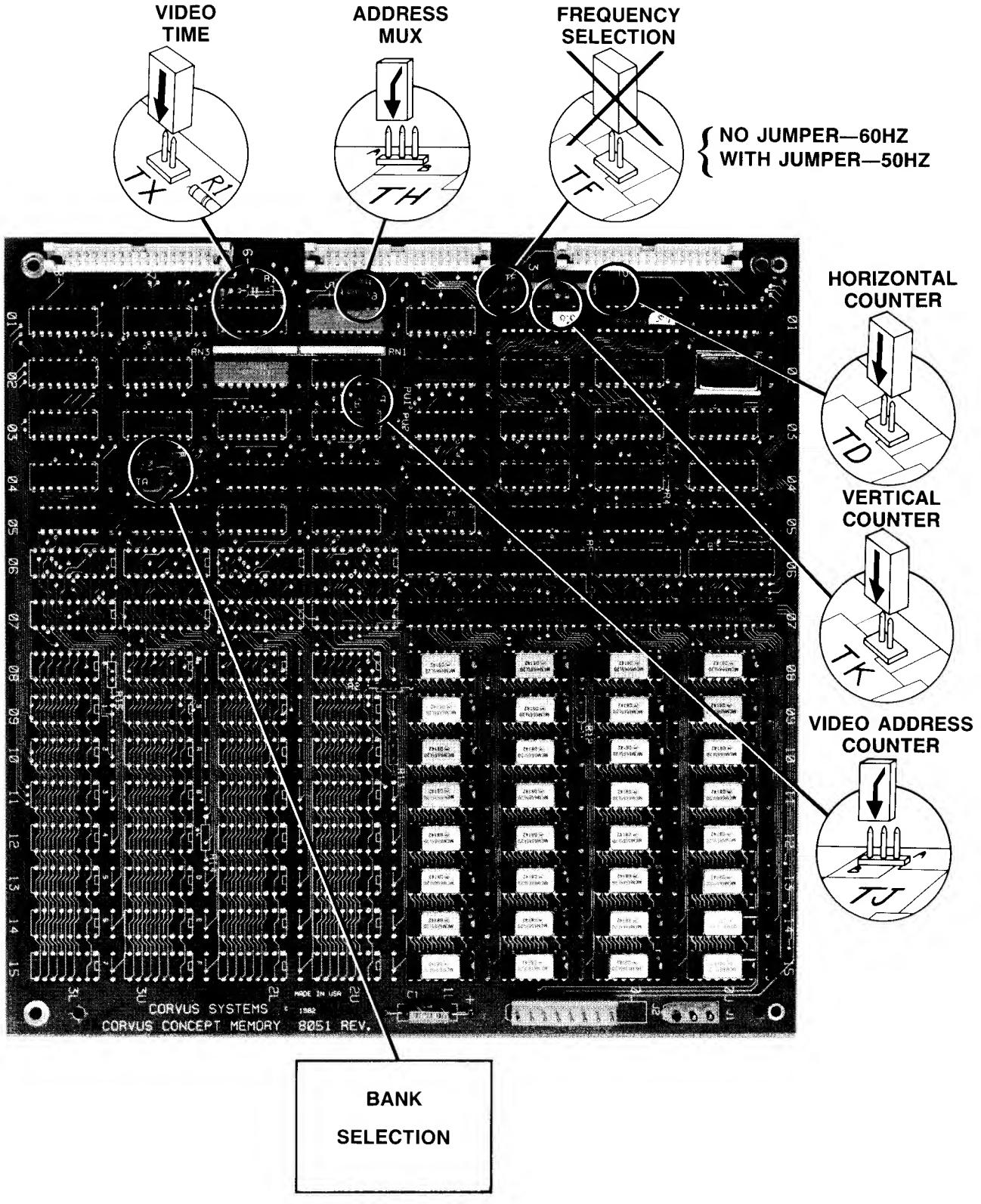
E

* Board level testers may jumper WRITE this pin instead of A22

** This pin is ALTMAP. It should always be zero for Concept. It can be jumpered.

APPENDIX G
MEMORY BOARD JUMPER LAYOUT


VIDEO TIME
ADDRESS MUX
FREQUENCY SELECTION
NO JUMPER—60HZ
WITH JUMPER—50HZ
HORIZONTAL COUNTER
VERTICAL COUNTER
VIDEO ADDRESS COUNTER
BANK SELECTION
TX
R1
TH
TF
TD
TK
TJ
CORVUS SYSTEMS
CORVUS CONCEPT MEMORY 8051 REV.


VIDEO TIME
ADDRESS MUX
FREQUENCY SELECTION
NO JUMPER—60HZ
WITH JUMPER—50HZ
HORIZONTAL COUNTER
VERTICAL COUNTER
VIDEO ADDRESS COUNTER
BANK SELECTION
CORVUS SYSTEMS
CORVUS CONCEPT MEMORY 8051 REV.

APPENDIX H
CONNECTOR

APPENDIX H-1
50-PIN I/O SLOT DESCRIPTION

Pin	Name	Description
1	NIOX	This line is normally high. When IOSLOT X is referenced, this line goes low. It can drive 20 LSTTL loads.
2-17	A1-A16	The buffered address bus. These address lines are always driven, and can supply 20 LSTTL loads from an I/O card.
18	NWRITE	This line goes low before 1M goes low, when the microprocessor writes to the I/O card. It remains low until after the cycle has occurred. NWRITE can drive 20 LSTTL loads total.
19	OPEN	
20	NIOSTB	This line goes low when an odd address between $39FE1 and $39FFF is selected.
21	OPEN	This is not READY.
22	OPEN	This is not DMA.
23	INTOUTX	Daisy chained interrupt line.
24	DMAOUTX	DMA daisy chain, could be used for IO card priority. DMA is NOT IMPLEMENTED!
25	+5V	500mA total current is available for all I/O cards.
26	Ground	System Electric Ground
27	DMAIN	Daisy chained DMA (DMA is not implemented)
28	INTIN	Daisy chained interrupt priority in.
29	NNMIX	'Non Maskable Interrupt' X. When the MC68000 interrupt priority is zero, a zero on this line will cause an interrupt. The source of the interrupt can then be determined by reading NSLOTMT.
30	NIRQX	Interrupt request. Similar function to NNMIX
31	NRESET	This line is pulled low by the processor power-on-reset signal. It should not be pulled low by the I/O card. If the I/O card pulls on this line some circuits are reset but the indeterminate.
32	OPEN	
33	−12V	200 mA per card
34	−5V	100 mA per card
35	OPEN	
36	8M	8.182 MHz (not 7.15 MHz)
37	Q3	assymetric 2.0455 MHz
38	N1M	1.02275 MHz clock, inverse of 1M
39		Common pullup
40	1M	1.02275 MHz clock
41	NDEVX	This line goes low to address registers on I/O cards. It can drive TTL loads. It is low only when N1M is high.
42-49	DI00-DI07	Bidirectional data lines. These lines are buffered except when the microprocessor reads from the I/O slot.
50	+12V	200 mA per card

APPENDIX H-2
DATA COMMUNICATION PORTS J1 AND J2

APPENDIX H-2
DATA COMMUNICATION PORTS J1 AND J2

Pin	V.24	RS-232C	Function
1	101	AB	Protective Ground
2	103	BA	Transmitted Data
3	104	BB	Received Data
4	105	CA	Request to Send
5	106	CB	Clear To Send
6	107	CC	Data Set Ready
7	102	AB	Signal Ground
8	109	CF	Data Carrier Detect
20	108	CD	Data Terminal Ready
23	111	CH	Data Signal Rate select (high/low Baud Rate dual speed modems)

All other pins are open.

APPENDIX H-3
BOARD CONNECTORS J4, J5, AND J6

APPENDIX H-3
BOARD CONNECTORS J4, J5, AND J6

Pin	J4 Name	J5 Name	J6 Name
1	Gnd	Gnd	Gnd
2	RA17	DOF	N16M
3	+5V	+5V	RA23
4	RA16	DOE	N8M
5	Gnd	Gnd	Gnd
6	RA15	DOD	N1M
7	+5V	+5V	+5V
8	RA14	DOC	RAMINT
9	Gnd	Gnd	Gnd
10	RA13	DOB	NRAM1
11	+5V	+5V	RA21
12	RA12	AOB	RA20
13	Gnd	Gnd	Gnd
14	RA11	DO9	RA19
15	+5V	+5V	RA22
16	RA10	DO8	NRAMACK
17	Gnd	Gnd	Gnd
18	RA9	DO7	RAMSEL
19	+5V	+5V	+5V
20	RA8	DO6	VA17
21	Gnd	Gnd	Gnd
22	RA7	DO5	VA18
23	+5V	+5V	+5V
24	RA6	DO4	VIDOFF
25	**Gnd**	**Gnd**	**Gnd**
26	**RA5**	**DO3**	**RNLDS**
27	+5V	+5V	+5V
28	RA4	DO2	NWRITEX
29	Gnd	Gnd	Gnd
30	RA3	DO1	NPARITYSELECT
31	+5V	+5V	+5V
32	RA2	DO0	XNRESET
33	Gnd	Gnd	Gnd
34	RA1	RA18	RNUDS

APPENDIX H-4
ADDITIONAL CONNECTORS

APPENDIX H-4
ADDITIONAL CONNECTORS

OMNINET Connector J3

J3 has 3 pins. The center pin is shield, the outer two push-pull balance signal lines between 0 and 5V.

Speaker and Battery Connector J5

Pin	Description
1	Speaker
2	+5V
3	Battery
4	Gnd

PCA Power Connector J8

Pin	Description
1	Shield
2	Ground
3	+5V
4	+12V
5	−12V
6	Open

Keyboard and Orientation Switch Connector J9

Pin	Description
1	Ground
2	Orientation switch
3	Keyboard data out
4	+5V
5	Keyboard data in
6	Ground
7	Open
8	Shield

APPENDIX I
CONCEPT PARTS LIST

APPENDIX I
CONCEPT SPARES

DESCRIPTION	PART NO.
MONITOR	8010-08082
KEYBOARD	8010-08083
ELECTRONICS DRAWER 512K	8010-08670
PROCESSOR BOARD	8010-08024
256K MEMORY BOARD	8010-08051
512K MEMORY BOARD	8010-08546
POWER SUPPLY	8010-08522
BIFORCATED CABLE	6010-02007
AC PANEL ASSY.	8010-08091
DC HARNESS	8010-08520
BATTERIES	4000-02982
RIBBON CABLES	8010-08523
MONITOR FRONT BEZEL	3100-01881
BASE TOP FOAM	3100-01889
BASE BOTTOM FOAM	3100-01890
FRONT PANEL FOAM	3100-01891
SWIVEL PLATE	3100-01896
MUFFIN FAN	2600-02080
MC68000 PROCESSOR	3265-01492
H BOOT ROM 2716	8105-09411
L BOOT ROM	8105-09412
UARTS (S46551)	3210-01472
VIA UART	3210-01473
H MACSBUG ROM	8105-09534
L MACSBUG ROM	8105-09535
MONOCHIP	8115-03023
MC68A54 IC	3210-01274
6801 V8.A IC	3265-02762
MEMORY MAPPER	8105-09011
HORIZONTAL COUNTER	8110-02076
VERTICAL COUNTER	8110-02944
75174 DRIVER	3210-01271
75175 RECEIVER	3210-01272
STATIC RAMS	3250-01458
DYNAMIC RAM	3255-01370
MEMORY UPGRADE	
ALLEN 4-40 X ¼	2800-01867
ALLEN 10-32 X 2½	2800-02151
LOCKWASHER #6	2800-01191
HEX ALLEN 6-32 X ½	2800-02234
HEX ALLEN 6-32 X ⅜	2800-01177
ALLEN 8-32 X ½	2800-01186
ALLEN 10-32 X ¼	2800-01859
STANDOFF 6-32	2850-02016
RIGHT GRIPLATCH	2800-02019
LEFT GRIPLATCH	2800-02018
SERVICE MANUAL	7100-04701
CONCEPT ADMINISTRATION MANUAL	7100-04699
SERVICE DISKETTE	7100-04699
CONCEPT BINDER	7200-04616
DEALER REPAIR TAGS	7200-04618

APPENDIX J
SPECIFICATIONS

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Microprocessor
- Motorola MC68000
- 32-Bit Data Registers
- 24-Bit Memory Address Bus

Memory
- 256 Kbytes Standard
- 512 Kbytes Optional

Input/Output
- OMNINET Network Interface
- Two Serial Asynchronous Controllers
- Clock/Calendar with Battery Backup
- Flexible Sound Generator with Speaker
- Two interval Timers

Video Monitor
- 15-Inch CRT (35MHz)
- Bit Mapped Display
- 720 Pixels by 560 Pixels
- 120 Characters by 56 Lines in Landscape Mode
- 90 Characters by 72 Lines in Portrait Mode
- Software Generated Character Set

Keyboard
- 91 Key Detached Keyboard
- Selectric R Style Keyboard
- 15 Keyboard Numeric Keypad
- 10 Programmable Function Keys
- Cursor Control Keys

Operating Systems and Software
- UCSD Pascal File Structure
- ISO Pascal with UCSD Extensions (Native Code Compiler)
- FORTRAN '77 (Native Code Compiler)
- 68000 Assembler
- EdWord™ Word Processor
- LogiCalc™ Electronic Spread Sheet
- CP/M Compatability

Electrical Specifications
- 100/120 or 220/240 Volts AC, Selectable
- 50 or 60 Hz
- 200 Watts

Physical Dimensions	**Height (in/cm)**	**Depth (in/cm)**	**Width (in/cm)**	**Weight (lbs/kg)**
Video Monitor	14/35.6	15/38.1	15/38.1	41/18.6
Base	4.5/11.4	15/38.1	17/43.2	24.5/11.2
Keyboard	3/7.6	8/20.3	17/43.2	4.7/2.1
Total Unit (Without Keyboard)	21/53.3	15/38.1	17/43.2	65.5/29.8